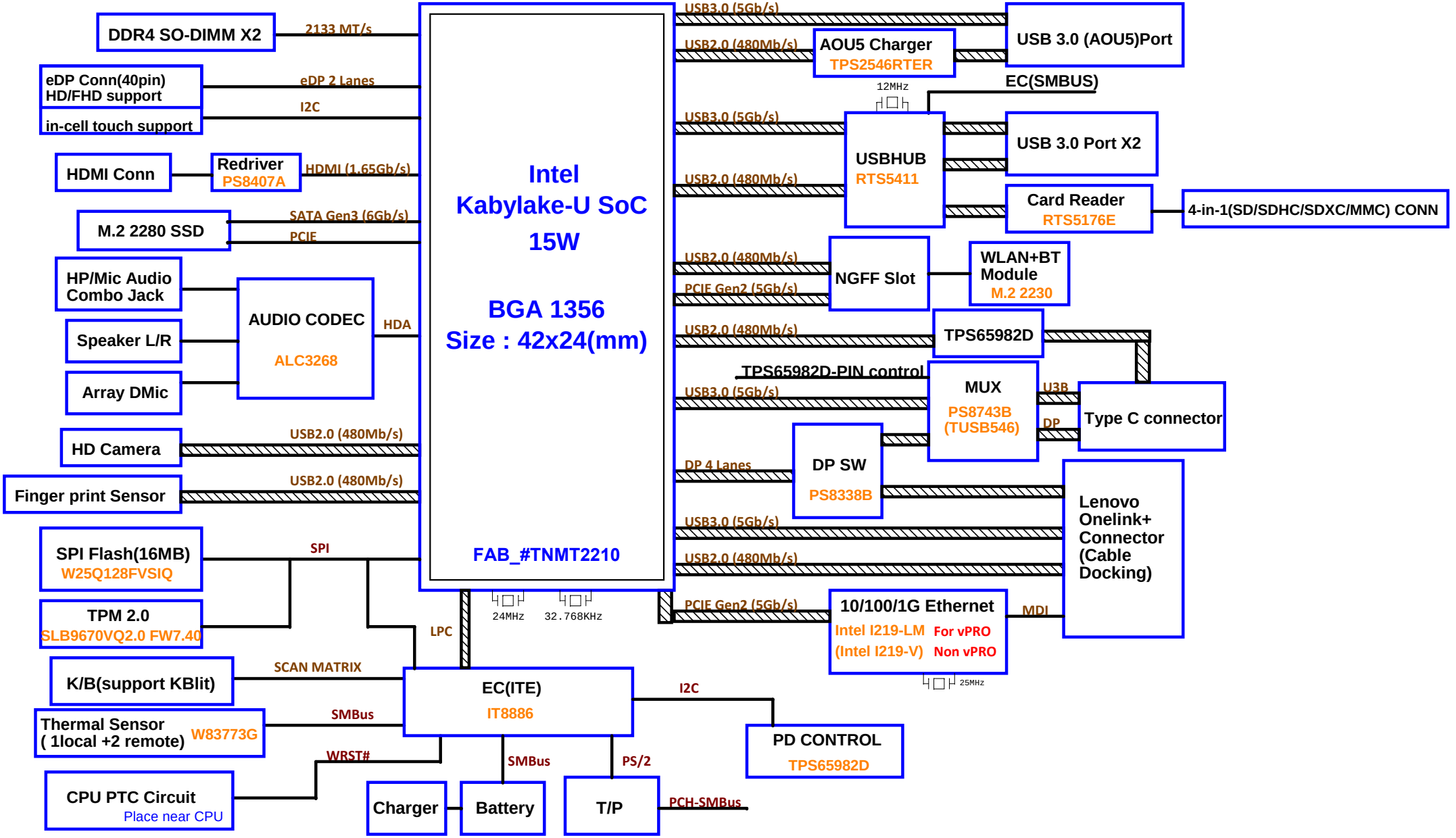
Bell2_Intel Kabylake-U Platform UMA Block Diagram (Windows)



www.schematic-x.blogspot.com

Quanta Computer Inc.
PROJECT: PS9
01 -- Bell Block Diagram
Wednesday, July 27, 2016

4,10,11,12,13,14,15,16,17,18,19,20,22,24,27,29,30,31,34,37,39,43,49 +3V
4,6,16,49,52 +VCCIO
4,5,6,9,43,49,52 +VCCSTPLL

HDMI

DOCK DP

U28A SKL_ULT ?

Need apply PN

20 IN_D2# → IN_D2# E55
20 IN_D2 → IN_D2 F55
20 IN_D1# → IN_D1# E58
20 IN_D1 → IN_D1 F58
20 IN_D0# → IN_D0# F53
20 IN_D0 → IN_D0 G53
20 IN_CLK# → IN_CLK# F56
20 IN_CLK → IN_CLK G56

34 DOCK_DDI2_TXN0 → DOCK_DDI2_TXN0 C50
34 DOCK_DDI2_TXP0 → DOCK_DDI2_TXP0 D50
34 DOCK_DDI2_TXN1 → DOCK_DDI2_TXN1 C52
34 DOCK_DDI2_TXP1 → DOCK_DDI2_TXP1 D52
34 DOCK_DDI2_TXN2 → DOCK_DDI2_TXN2 A50
34 DOCK_DDI2_TXP2 → DOCK_DDI2_TXP2 B50
34 DOCK_DDI2_TXN3 → DOCK_DDI2_TXN3 D51
34 DOCK_DDI2_TXP3 → DOCK_DDI2_TXP3 C51

DDI1_TXN[0] DDI1_TXP[0] DDI1_TXN[1] DDI1_TXP[1] DDI1_TXN[2] DDI1_TXP[2] DDI1_TXN[3] DDI1_TXP[3]
DDI2_TXN[0] DDI2_TXP[0] DDI2_TXN[1] DDI2_TXP[1] DDI2_TXN[2] DDI2_TXP[2] DDI2_TXN[3] DDI2_TXP[3]
DDI
EDP

EDP_TXN[0] C47 INT_EDP_TXN0 → INT_EDP_TXN0 19 / INT_EDP_TXP0 19
EDP_TXP[0] C46 INT_EDP_TXP0
EDP_TXN[1] D46 INT_EDP_TXN1 → INT_EDP_TXN1 19 / INT_EDP_TXP1 19
EDP_TXP[1] C45 INT_EDP_TXP1
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

EDP_AUXN E45 INT_EDP_AUXN → INT_EDP_AUXN 19 / INT_EDP_AUXP 19
EDP_AUXP F45 INT_EDP_AUXP

EDP_DISP_UTIL B52

DDI1_AUXN G50
DDI1_AUXP C50
DDI2_AUXN C48 DOCK_DDI2_AUXN → DOCK_DDI2_AUXN 34 / DOCK_DDI2_AUXP 34
DDI2_AUXP F48 DOCK_DDI2_AUXP
DDI3_AUXN G46
DDI3_AUXP C46

20 SDVO_CLK → L13
20 SDVO_DATA → L12
GPP_E18/DDPB_CTRLCLK
GPP_E19/DDPB_CTRLDATA

+3V → R721 2.2K_4 → N7
N8
GPP_E20/DDPC_CTRLCLK
GPP_E21/DDPC_CTRLDATA

N11
TP47 → N12
GPP_E22/DDPD_CTRLCLK
GPP_E23/DDPD_CTRLDATA

+VCCIO → R242 24.9/F_4 → EDP_RCOMP E52
EDP_RCOMP

GPP_E13/DDPB_HPD0 L9 PCH_HDMI_HPD → PCH_HDMI_HPD 20
GPP_E14/DDPC_HPD1 L7 PCH_DOCK_DP_HPD → PCH_DOCK_DP_HPD 34
GPP_E15/DDPD_HPD2 L6
GPP_E16/DDPE_HPD3 N9
GPP_E17/EDP_HPD C10 EDP_HPD → EDP_HPD 19

EDP_BKLTEN R12 PCH_LVDS_BLON → PCH_LVDS_BLON 19
EDP_BKLTCTL R11 PCH_DPST_PWM → PCH_DPST_PWM 19
EDP_VDDEN U13 PCH_LCDVCC_EN → PCH_LCDVCC_EN 19

DISPLAY SIDEBANDS

KBL-ULT
REV = 1
1 OF 20 ?

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Reserve EDP_HPD opposites circuit!

+3V → R424 → 10K_4 → EDP_HPD
R418 → 100K_4

+VCCSTPLL → PM_THRMTRIP# R487 1K_4

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL .
470 OHM IS FOR I/P

U28D SKL_ULT ?

Need apply PN

TP37
29 EC_PECI → EC_PECI A54
CATERR# D63
PECI
PROCHOT# C65
THERMTRIP# C63
SKTOCC# A65

29,41,43 H_PROCHOT# → R511 499/F_4 → PROCHOT# C65
29 PM_THRMTRIP# → PM_THRMTRIP# C63

CPU MISC

16 XDP_BPM0 → BPM#[0] C55
16 XDP_BPM1 → BPM#[1] D55
BPM#[2] B54
BPM#[3] C56

19 TOUCH_I2C_INT# → TP48 → GPP_E3/CPU_GP0 A6
GPP_E7/CPU_GP1 A7
GPP_B3/CPU_GP2 BA5
GPP_B4/CPU_GP3 AY5

R89 49.9/F_4 → PROC_POPIRCOMP AT16
R79 49.9/F_4 → PCH_OPI_RCOMP AU16
R241 49.9/F_4 → EDRAM_OPIO_RCOMP H66
R237 49.9/F_4 → EOPIO_RCOMP H65

PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

JTAG

PROC_TCK B61 XDP_TCK0 → XDP_TCK0 16
PROC_TDI D60 XDP_TDI_CPU → XDP_TDI_CPU 16
PROC_TDO A61 XDP_TDO_CPU → XDP_TDO_CPU 16
PROC_TMS C60 XDP_TMS_CPU → XDP_TMS_CPU 16
PROC_TRST# B59 XDP_TRST#_CPU

PCH_JTAG_TCK B56 JTAG_TCK_PCH → JTAG_TCK_PCH 16
PCH_JTAG_TDI D59 JTAG_TDI_PCH → JTAG_TDI_PCH 16
PCH_JTAG_TDO A56 JTAG_TDO_PCH → JTAG_TDO_PCH 16
PCH_JTAG_TMS C59 JTAG_TMS_PCH → JTAG_TMS_PCH 16
PCH_TRST# C61 XDP_TRST#_CPU → XDP_TRST#_CPU 16
JTAGX A59 JTAGX_PCH → JTAGX_PCH 16

KBL-ULT
REV = 1
4 OF 20

PLACE NEAR CPU

+VCCIO → XDP_TDO_CPU R486 100_4

+VCCSTPLL → H_PROCHOT# R516 1K_4
XDP_TCK0 R485 51_4

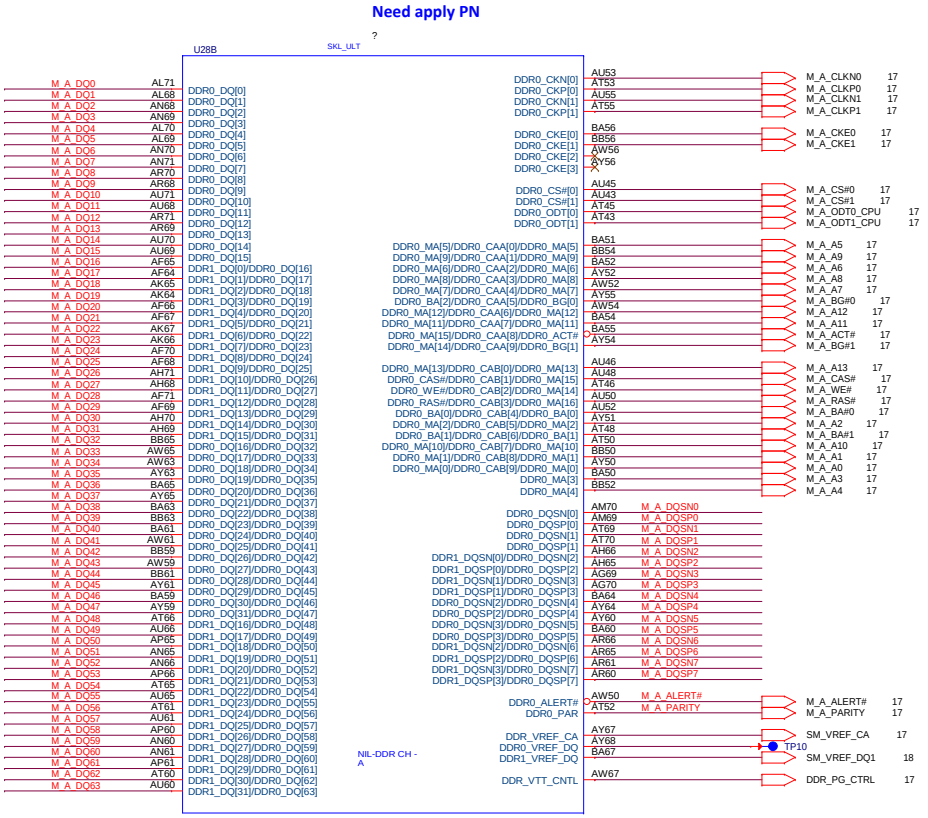
+VCCIO → R505 0_4
R508 51_4 → JTAG_TMS_PCH
R494 51_4 → JTAG_TDI_PCH
R507 100_4 → JTAG_TDO_PCH
R493 *51_4 → JTAG_TCK_PCH

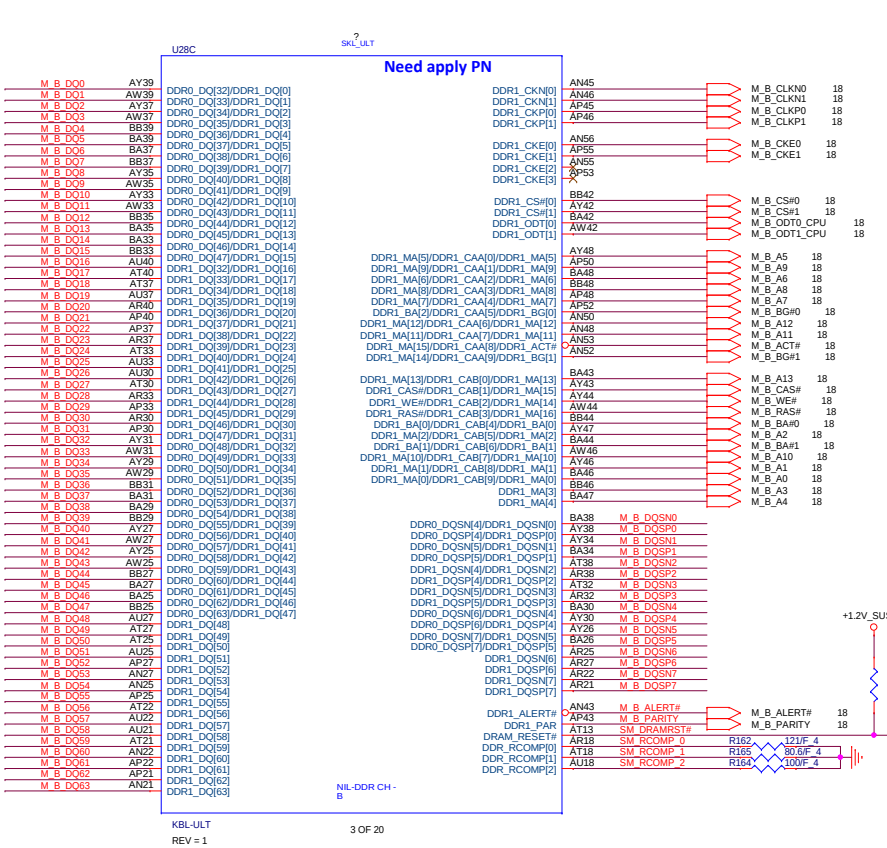
Close to Chipset

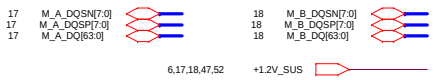
Quanta Computer Inc.
PROJECT: PS9

Size	Document Number	Rev
	Custom 02 -- KABYLAKE 1/15(eDP/DDI)	1A
Date: Wednesday, July 27, 2016	Sheet 2 of 55	

KabyLake ULT Processor (DDR4)







Quanta Computer Inc.			
PROJECT: PS9			
Size	Document Number Custom	03 -- KABYLAKE 2/15(DDR3-A I/F)	Rev 1A
Date: Wednesday, July 27, 2016	Sheet 3 of 55		

10,11,14,15,16 +3V_DEEP_SUS
10,12,15,16,19,21,23,25,27,28,31,32,36,37,42,48,49,50,52 +3VS5
2,10,11,12,13,14,15,16,17,18,19,20,22,24,27,29,30,31,34,37,39,43,49 +3V
19,26,27,28,32,33,37,42,43,46,47,48,49,50,52 +5VS5
2,6,16,49,52 +VCCIO
2,5,6,9,43,49,52 +VCCSTPLL
13,15 +3V_RTC_2

U28K SKL_ULT ?

SYSTEM POWER MANAGEMENT

Need apply PN

GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
PROCPWRGD
VCCST_PWRGD
SYS_PWROK
PCH_PWROK
DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDNACK
GPP_A15/SUSACK#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPD7/RSVD

GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
SLP_SUS#
SLP_LAN#
GPD9/SLP_WLAN#
GPD6/SLP_A#
GPD3/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#
GPP_A11/PME#
INTRUDER#
GPP_B11/EXT_PWR_GATE#
GPP_B2/VRALERT#

KBL-ULT
REV = 1
11 OF 20
?

16 SYS_RESET# / 16,29 RSMRST#
R447 *10K_4 PROCPWRGD / H_VCCST_PWRGD
C469 *0.1U/16V_4 SYS_PWROK / EC_PWROK
22,29,30 EC_PWROK
29 SUSPWRDNACK
*0_4 R129 SUSACK#
25 PCIE_WAKE#
23 LANWAKE#
23 LAN_DIS#
19 TOUCH_EN

PLTRST# AN10
SYS_RESET# B5
RSMRST# AY17
PROCPWRGD A68
H_VCCST_PWRGD B65
SYS_PWROK B6
EC_PWROK BA20
DSWROK_EC_R BB20
SUSPWRDNACK AR13
SUSACK# AP11
PCIE_WAKE# BB15
LANWAKE# AM15
LAN_DIS# AW17
AT15

AT11 PCH_SLP_S0_N
AP15
BA16
AY16
AN15
AW15
BB17
AN16
BA15 DNBSWON#
AY15 AC_PRESENT_EC
AU13 PM_BATLOW_N_EC
AU11
AP16 INTRUDER#_R R163 1M_4 +3V_RTC_2
AM10 EXT_PWR_GATE#
AM11

PCH_SLP_S0_N 16
SUSB# 16,29
SUSC# 16,29
SLP_S5# 16
SLP_LAN# 23
SLP_WLAN# 25
SLP_A# 16,29
DNBSWON# 16,29
AC_PRESENT_EC 29
PM_BATLOW_N_EC 29

RSMRST#
SYS_RESET#
EC7 *220P/50V_4
EC9 *220P/50V_4

RSMRST# R100 *0_4_S DSWROK_EC_R
PLTRST#
EC18 *220P/50V_4

PCH Pull-high/low(CLG)

+3V_DEEP_SUS
SUSPWRDNACK R114 *10K_4
SUSACK# R128 *10K_4
PM_BATLOW_N_EC R144 10K_4

+3VS5
PCIE_WAKE# R70 1K_4
AC_PRESENT_EC R84 10K_4
LANWAKE# R124 10K_4

+3V
SYS_RESET# R475 10K_4
RSMRST# R80 10K_4
DSWROK_EC_R R91 *100K/F_4
TOUCH_EN R815 100K/F_4
SYS_PWROK R862 *10K_4

EXT_PWR_GATE# R60 *20K/F_4 +3VS5

Close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"

+VCCIO +VCCSTPLL
R517 1K_4
R512 *1K_4
16,29,47,50 HWPG D24 1 2 DB2J40600L H_VCCST_PWRGD_R R491 60.4/F_4 H_VCCST_PWRGD
C495 *10P/50V_4

+VCCIO
R514 15K_4
C497 0.1U/16V/X7R
R500 100K_4

+5VS5
R520 100K_4
+1.0V_PWRGD_G1
+1.0V_PWRGD_G2 2
Q34 PMBT3904

+3VS5
R522 *10K_4
HWPG
Q36 DMN601K-7
R525 100K_4

21,23,24,25,29,30 PLTRST#
R224 100K/F_4

PLTRST#(CLG)

29 SYS_PWROK
SYS_PWROK R482 0_4 EC_PWROK
R476 100K/F_4

System PWR_OK(CLG)

Quanta Computer Inc.			
PROJECT: PS9			
Size: Custom	Document Number: 04 -- KABYLAKE 3/15(Power Manger)		Rev: 1A
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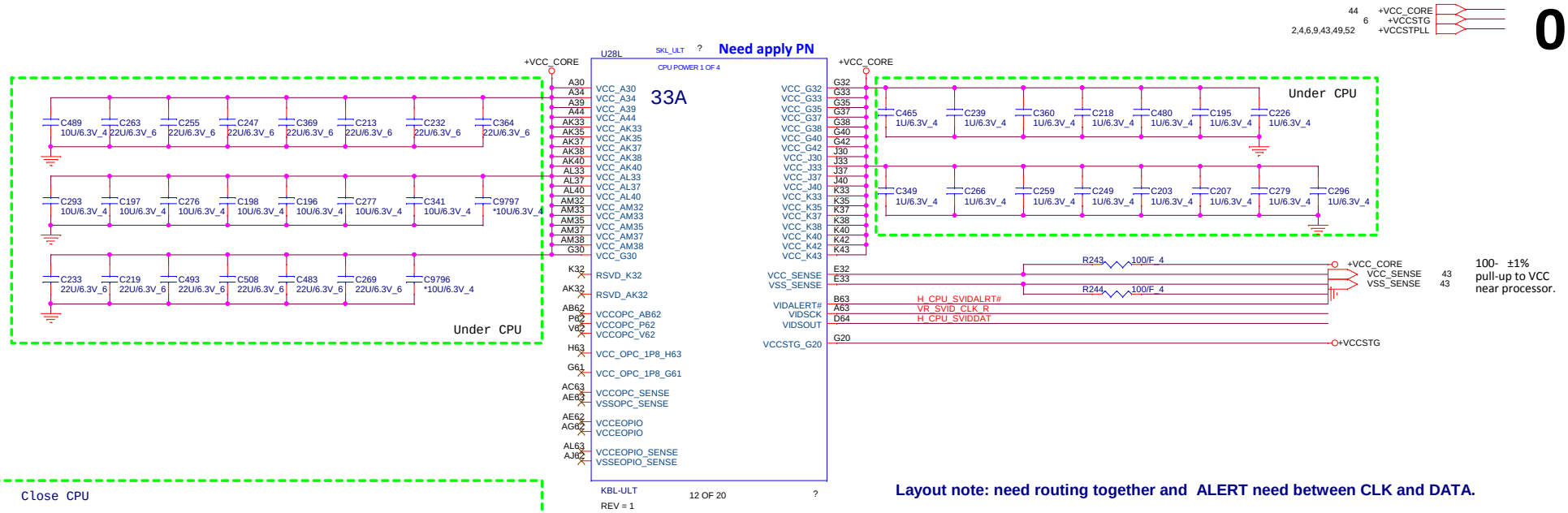

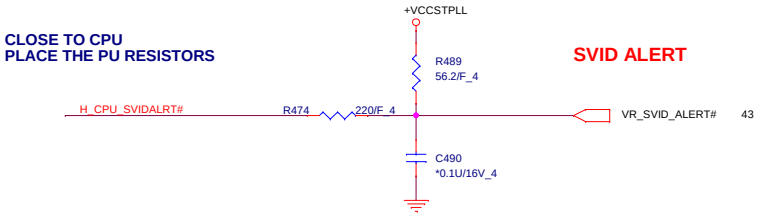

Layout note: need routing together and ALERT need between CLK and DATA.

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

Quanta Computer Inc.
PROJECT: PS9

Size	Document Number	Rev
	Custom 05 -- KABYLAKE 4/15 (POWER-1)	1A
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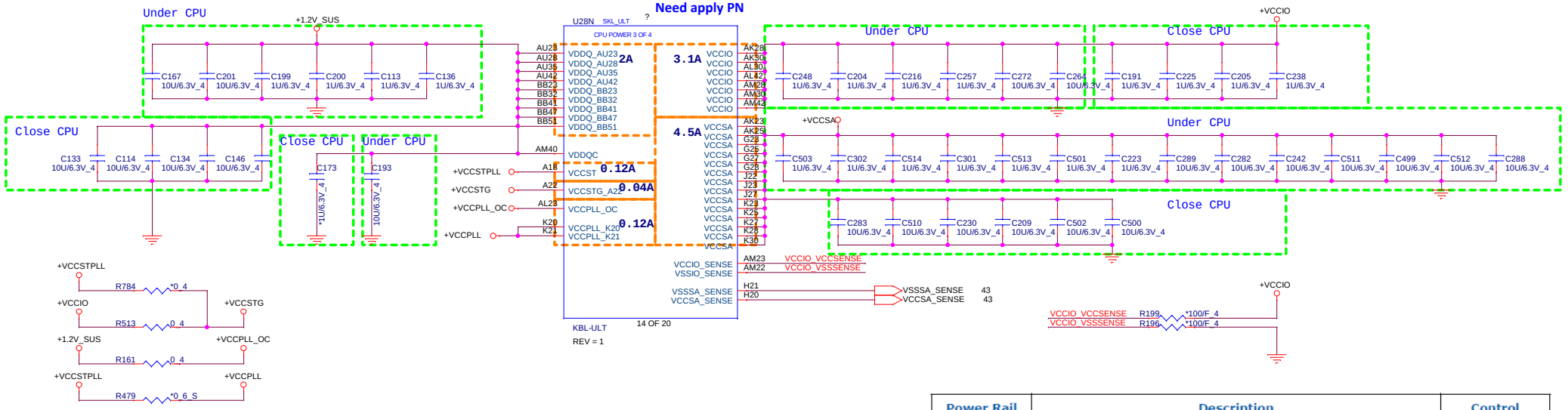
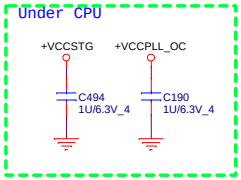
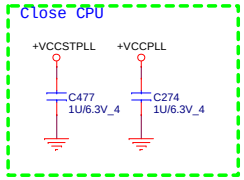
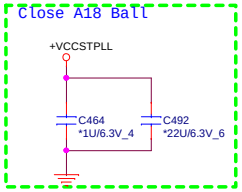
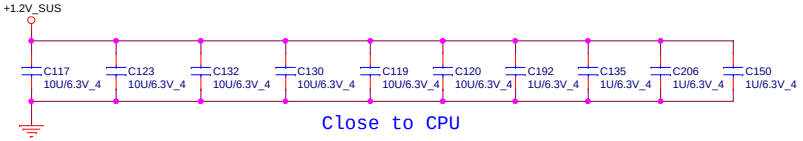






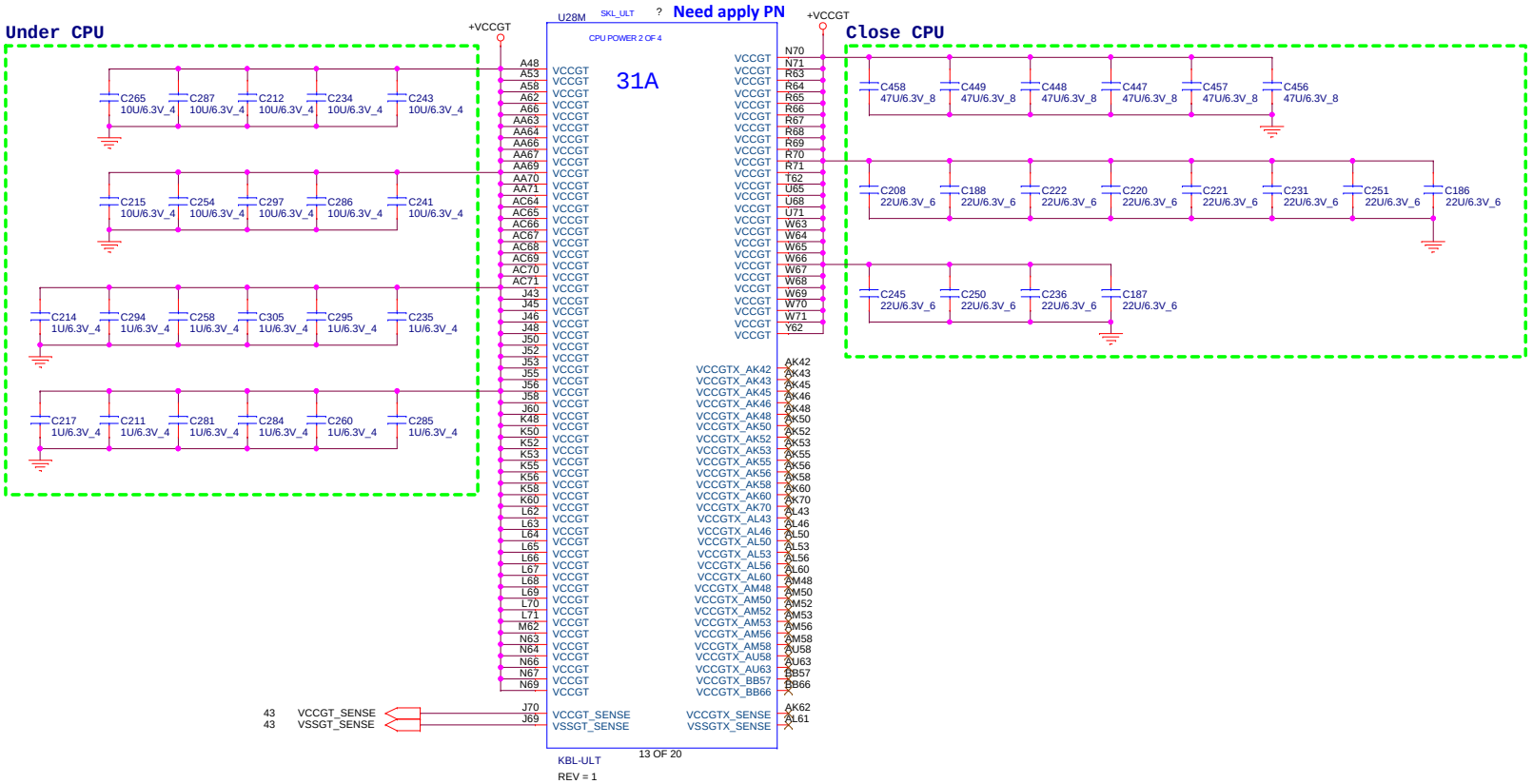




Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

Quanta Computer Inc.
PROJECT: PS9

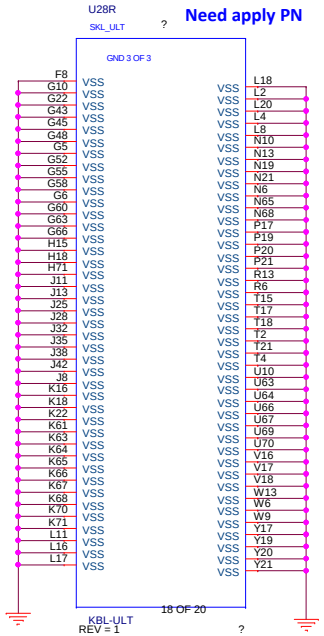
Size	Document Number	Rev
	Custom 06 -- KABYLAKE 5/15 (POWER-2)	1A
Date: Wednesday, July 27, 2016	Sheet 6 of 55	

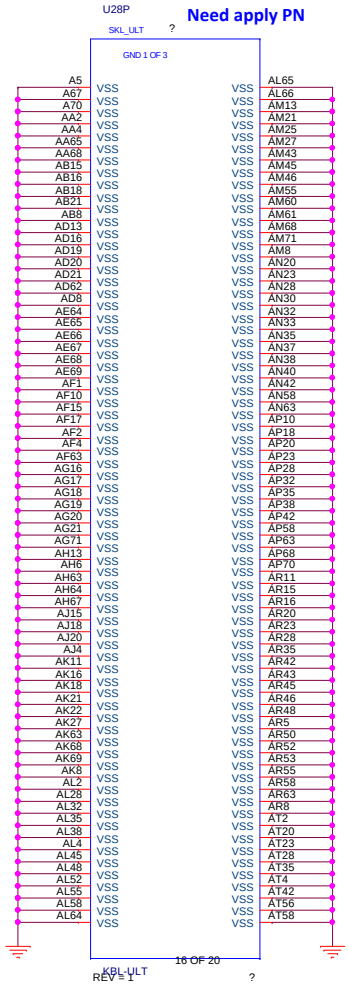


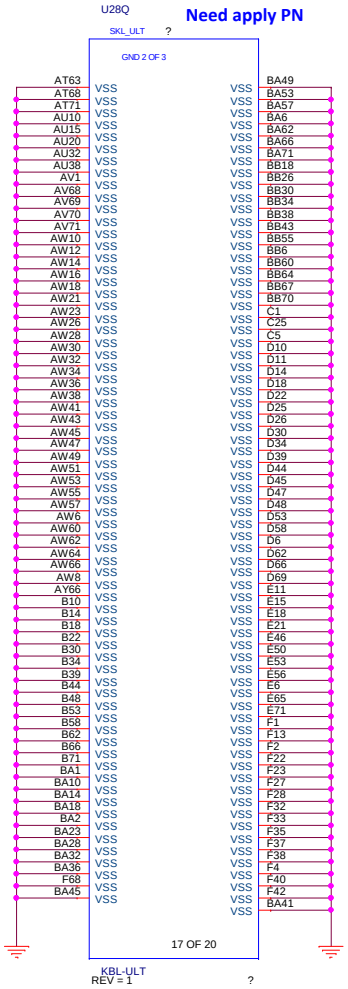
Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

Quanta Computer Inc.
PROJECT: PS9

Size	Document Number	Rev
	Custom 07 -- KABYLAKE 6/15 (POWER-3)	1A
Date: Wednesday, July 27, 2016	Sheet 7 of 55	





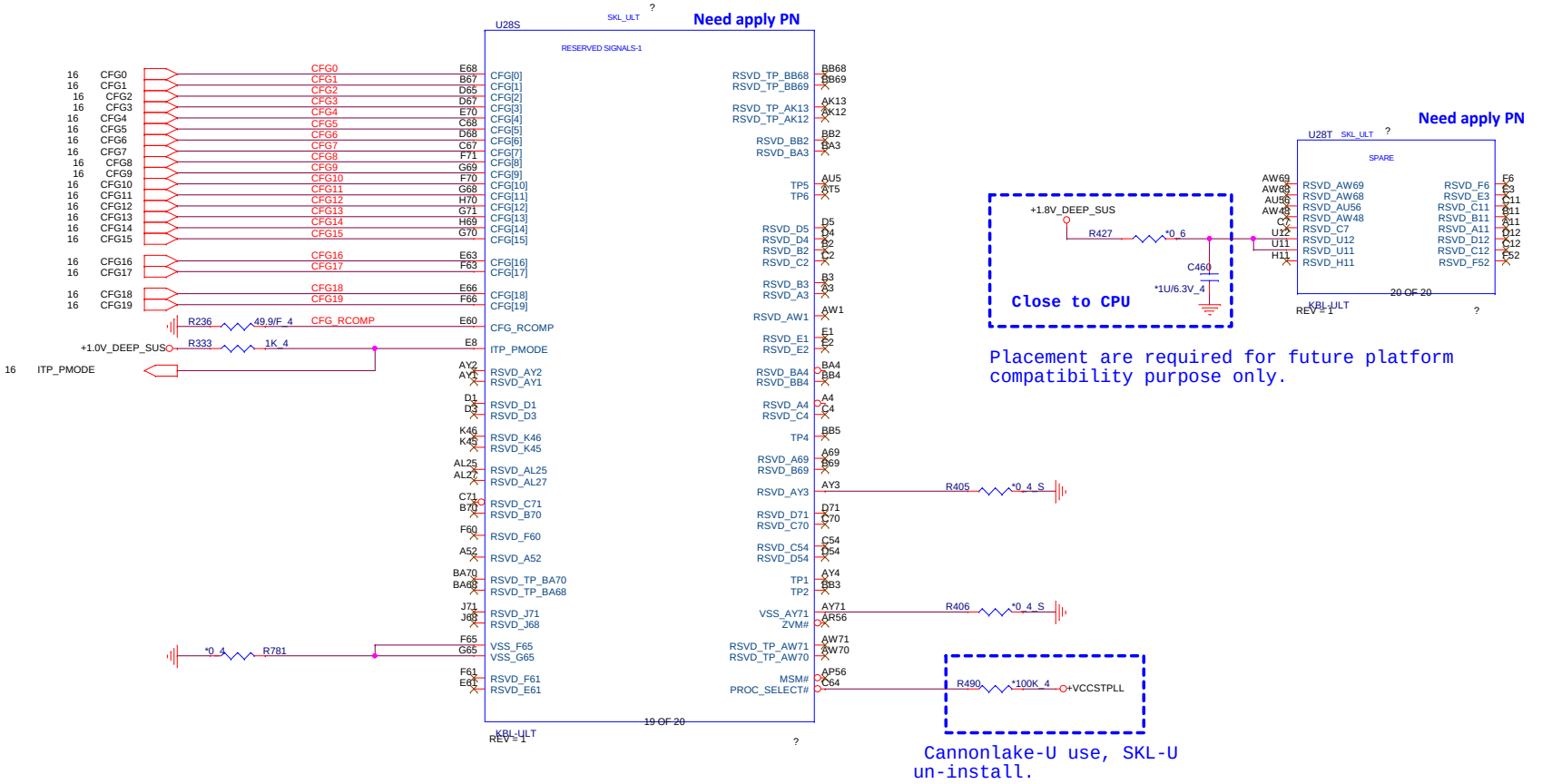


Quanta Computer Inc.

PROJECT: PS9

Size	Document Number Custom	Rev
	8 -- KABYLAKE 7/15 (GND)	1A
Date: Wednesday, July 27, 2016	Sheet 8 of 55	

13,15,16,48,49,52 +1.0V_DEEP_SUS
2,4,5,6,43,49,52 +VCCSTPLL
15,50,52 +1.8V_DEEP_SUS



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R440 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R439 1K_4

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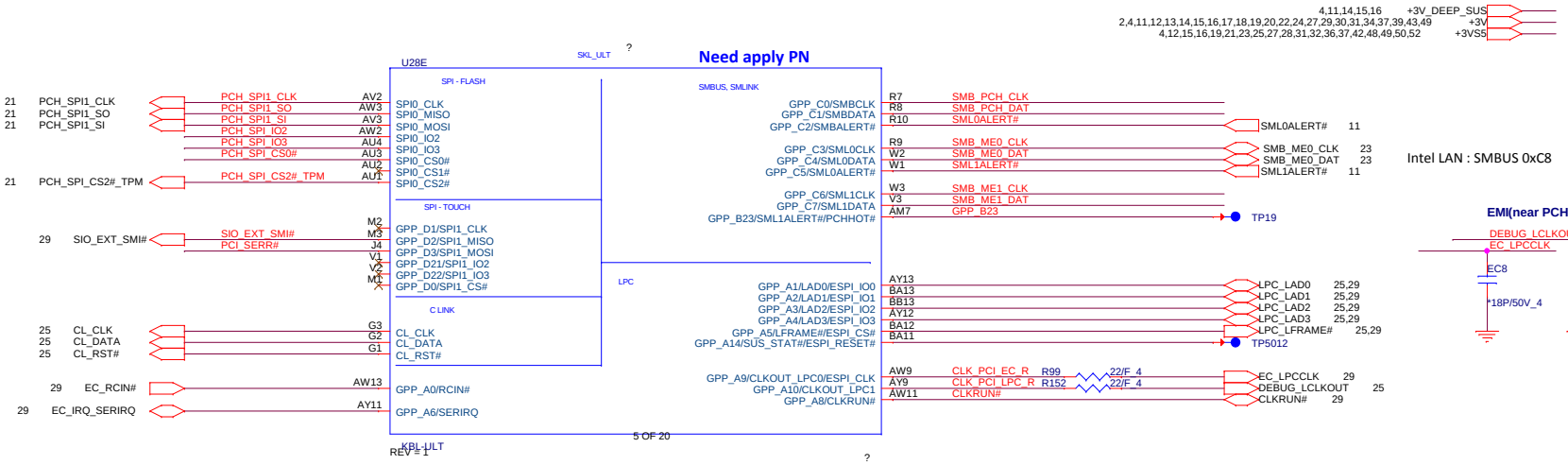
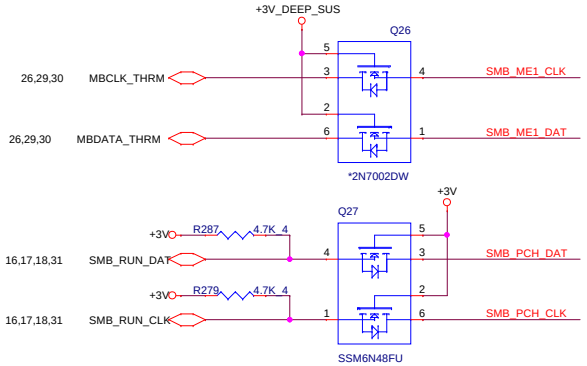
PROJECT: PS9

Size	Document Number	Rev
	Custom 9 -- KABYLAKE 8/15 (RSV)	1A
Date: Wednesday, July 27, 2016	Sheet 9 of 55	



GPIO Pull UP

SMBus/Pull-up(CLG)

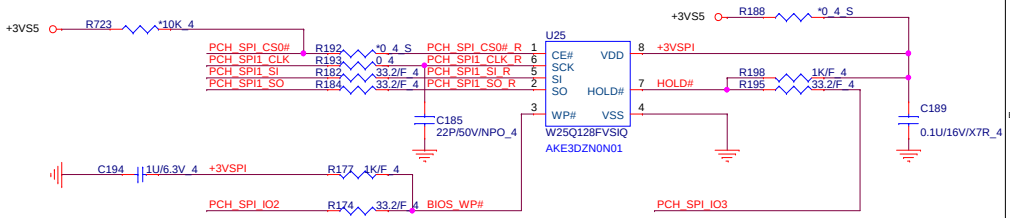


CPU heat pipe local thermal sensor
DDR thermal sensor
EC

Touch Pad
XDP
DDR3-L

PCH SPI ROM(CLG)

Need place to TOP



R1/R2/R3/R4/R5/R7 close to U15 pin

Vender	Size	P/N
MIT	16MB	AKE3DZN0L03(N25Q128A13ESEDFF)
Winbond	16MB	AKE3DZN0N01 (W25Q128FVSIQ)
MX	16MB	AKE3DZN0Z03(MX25L12873FM2I-10G)
Socket		DFHS08FS023

Quanta Computer Inc.
PROJECT: PS9

Size	Document Number	Rev
Custom	10 -- KABYLAKE 9/15(SPI/LPC/SMBUS)	1A
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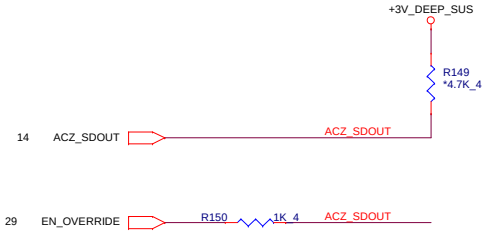
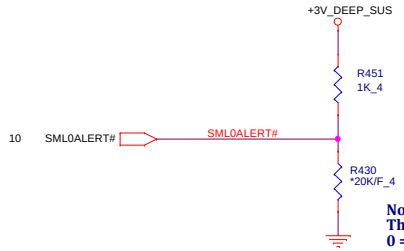
Functional Strap Definitions

DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET

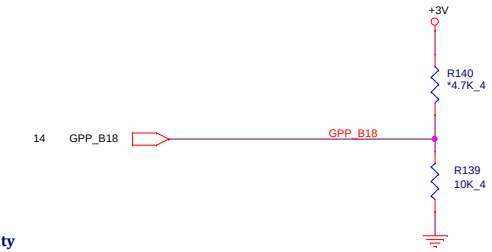
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



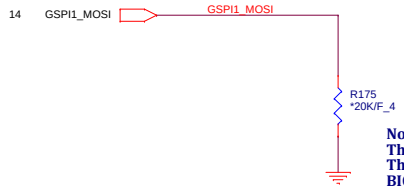
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

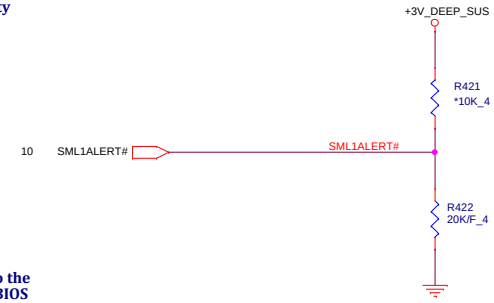


No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO
Timer system reboot feature).
This function is useful when running ITP/XDP.

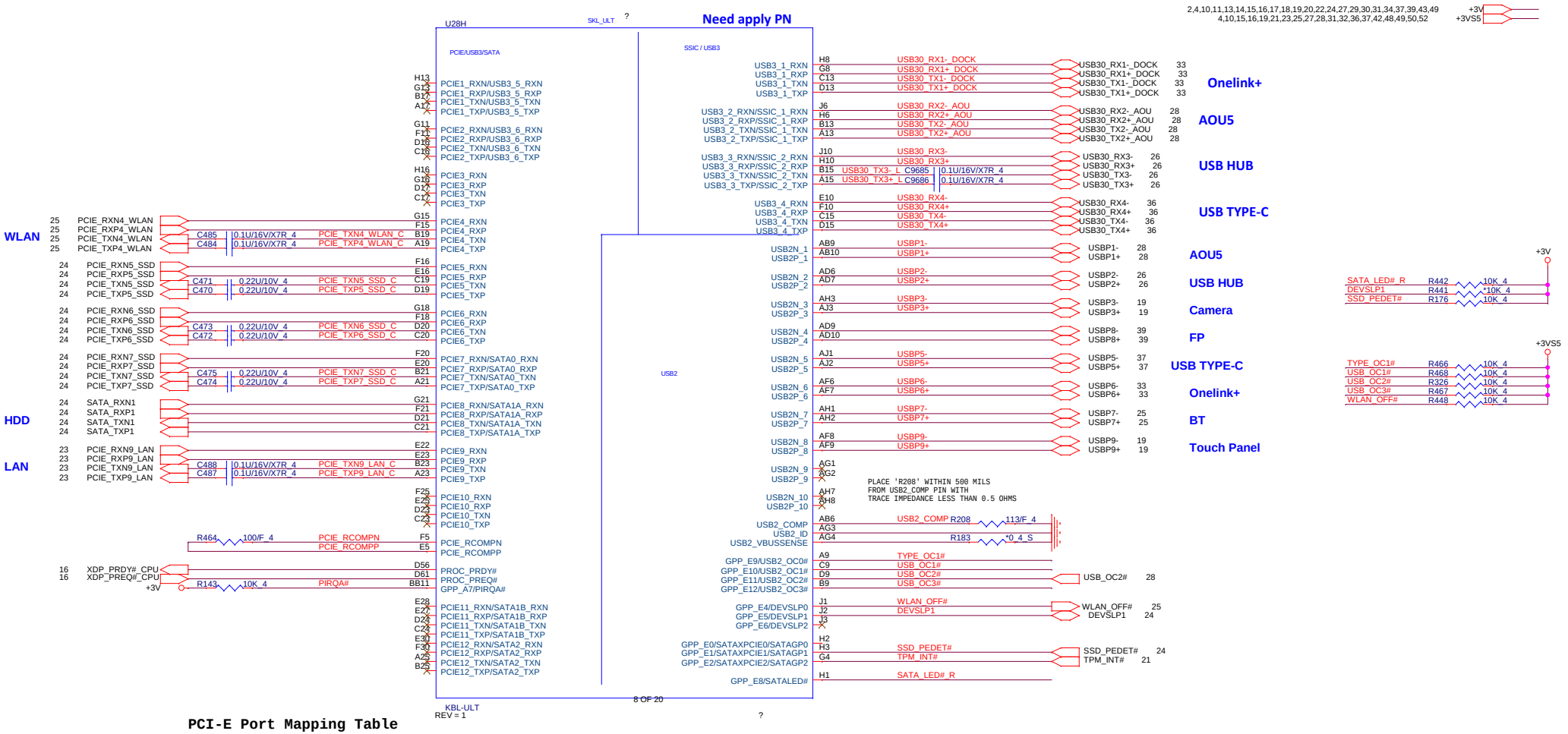


No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.



PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	Un-used	Port0	Un-used
Port2	Un-used	Port1	Un-used
Port3	Un-used	Port2	WLAN
Port4	WLAN	Port3	LAN
Port5	PCIESSD (Reseve)	Port4	SSD(Reserve)
Port6	PCIESSD (Reseve)	Port5	Un-used
Port7	PCIESSD (Reseve)		
Port8	HDD		
Port9	LAN		
Port10	Un-used		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	Onelink+
PORT-2	AOU5
PORT-3	USB HUB
PORT-4	USB TYPE-C

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	AOU5
PORT-2	USB HUB
PORT-3	Camera
PORT-4	Cardreader
PORT-5	TYPE C
PORT-6	Onelink+
PORT-7	BT
PORT-8	FP
PORT-9	Touch Panel
PORT-10	NC

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	Custom 12 -- KABYLAKE 11/15 (PCIE/USB)	1A
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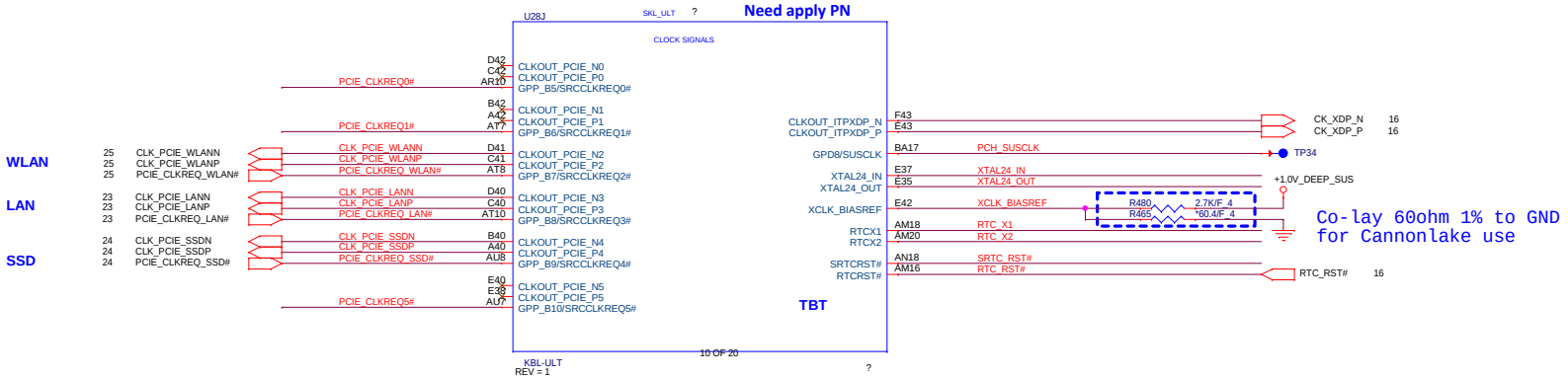
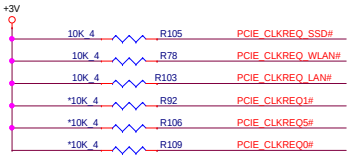
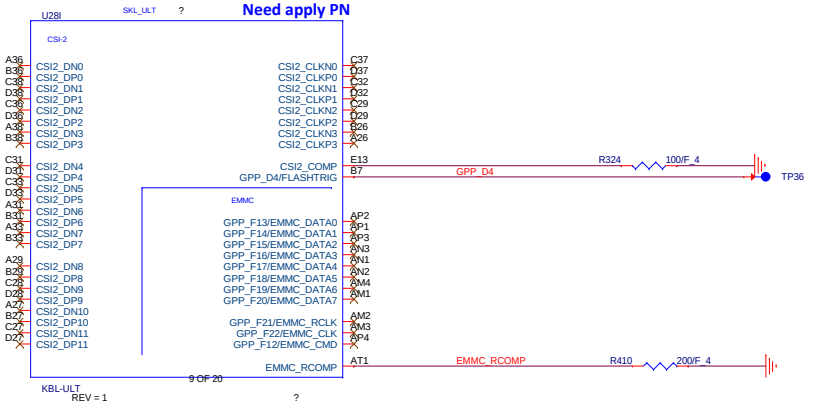
4,15 +3V_RTC_2
2,4,10,11,12,14,15,16,17,18,19,20,22,24,27,29,30,31,34,37,39,43,49 +3V
9,15,16,48,49,52 +1.0V_DEEP_SUS
19,22,25,29,32,33,37,41,42,53 +3VPCU

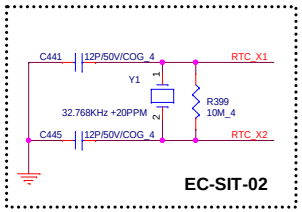


CLK_REQ/Strap Pin(CLG)



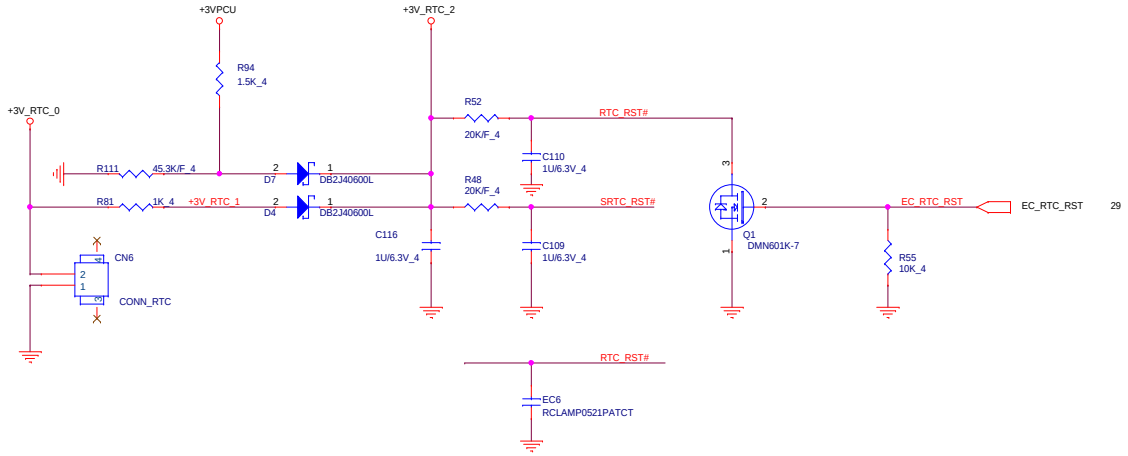


RTC Clock 32.768KHz



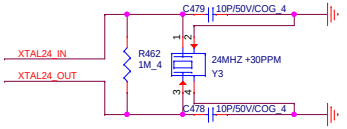
RTC Circuitry(RTC)

RTC Power trace width 20mils.



External Crystal and Green Clock

EC-SIT-31



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	Custom 13 KABYLAKE 12/15 (CLK/EMMC)	1A
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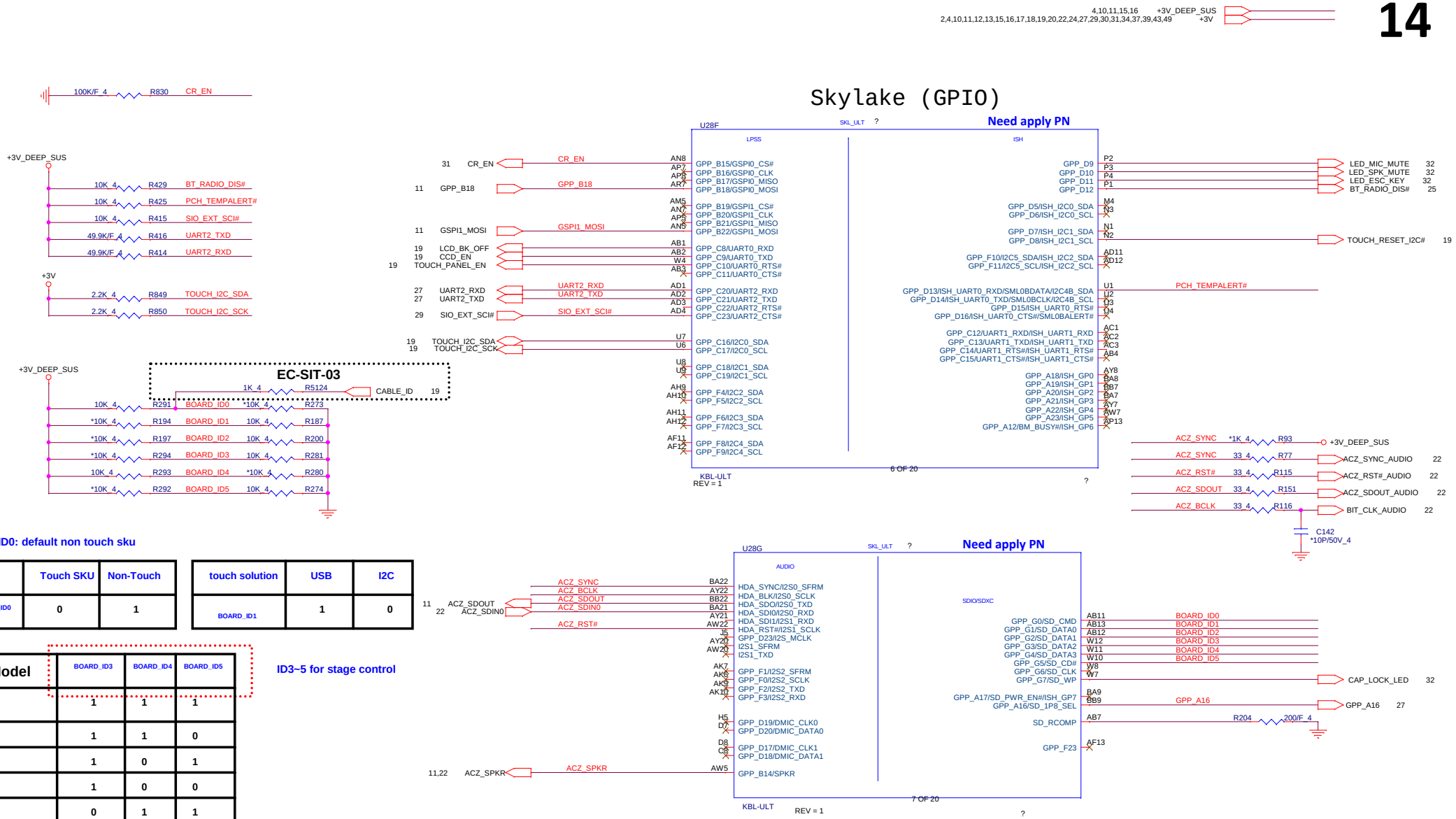
Skylake (GPIO)



ID0: default non touch sku

	Touch SKU	Non-Touch
BOARD_ID0	0	1

touch solution	USB	I2C
BOARD_ID1	1	0

Model	BOARD_ID3	BOARD_ID4	BOARD_ID5
	1	1	1
	1	1	0
	1	0	1
	1	0	0
	0	1	1
SIT	0	1	0
FVT	0	0	1
BU	0	0	0

ID3~5 for stage control

EC-FVT-03

Intel LAN	VPRO	n-VPRO
BOARD_ID2	1	0

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	Custom 14 -- KABYLAKE 13/15 (HDA/GPIO)	1A
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4,10,11,14,16 +3V_DEEP_SUS
9,13,16,48,49,52 +1.0V_DEEP_SUS
9,50,52 +1.8V_DEEP_SUS
4,10,12,16,19,21,23,25,27,28,31,32,36,37,42,48,49,50,52 +3VS5
4,13 +3V_RTC_2
2,4,10,11,12,13,14,16,17,18,19,20,22,24,27,29,30,31,34,37,39,43,49 +3V

U28O SKL_ULT
CPU POWER 4 OF 4
15 OF 20
KBL-ULT
REV = 1

Need apply PN

PCH Internal VRM

C820 and C690 close to cpu less then 100 mils

20mils

2.899A
2.57A
1.714A
0.03A
0.09A

VCCPRIM_1P0 AB19, AB20, P18
VCCPRIM_CORE AF18, AF19, V20, V21
DCPDSW_1P0 AL1
VCCMPHYAON_1P0 K17, L1
VCCMPHYGT_1P0 N15, N16, N17, P15, P16
VCCAMPHYPLL_1P0 K15, L15
VCCAPLL_1P0 V15
VCCPRIM_1P0_AB17 AB17, Y18
VCCSDSW_3P3_AD17 AD17, AD18, AJ17
VCCHDA AJ19
VCCSPI AJ16
VCCSRAM_1P0 AF20, AF21, T19, T20
VCCPRIM_3P3_AJ21 AJ21
VCCPRIM_1P0_AK20 AK20
VCCAPLLEBB N18
VCCPGPPA AK15
VCCPGPPB AG15
VCCPGPPC Y16
VCCPGPPD Y15
VCCPGPPE T16
VCCPGPPF AF16
VCCPGPPG AD15
VCCPRIM_3P3_V19 V19
VCCPRIM_1P0_T1 T1
VCCATS_1P8 AA1
VCCRTCPRIM_3P3 AK17
VCCRTC_AK19 AK19
VCCRTC_BB14 BB14
DCPRTC BB10
VCCCLK1 A14
VCCCLK2 K19
VCCCLK3 L21
VCCCLK4 N20
VCCCLK5 L19
VCCCLK6 A10
GPP_B0/CORE_VID0 AN11
GPP_B1/CORE_VID1 AN13

+VCCPRIM_1.0V_T1 R222 *0_6_S +1.0V_DEEP_SUS
+VCCATS_1.8V R407 *0_6_S +1.8V_DEEP_SUS
+VCCRTCPRIM_3.3V R390 *0_6_S +3V_DEEP_SUS
+VCCRTC R158 *0_4_S +3V_RTC_2
DCPRTC C164 0.1U/16V/X7R_4
+VCCCLK1 R470 *0_6_S +1.0V_DEEP_SUS
+VCCCLK2 R348 *0_6_S
+VCCCLK3 R341 *0_6_S
+VCCCLK4 R331 *0_6_S
+VCCCLK5 R337 *0_6_S
+VCCCLK6 R478 *0_6_S
C476 1U/6.3V_4
CORE_VID0 TP17
CORE_VID1 TP16
C453 1U/6.3V_4 +3V_DEEP_SUS

+3V_DEEP_SUS
+VCCPGPPA R385 *0_6_S
+VCCPGPPB R393 *0_6_S
+VCCPGPPC R216 *0_6_S
+VCCPGPPD R211 *0_6_S
+VCCPGPPE R218 *0_6_S
+VCCPGPPG R205 *0_6_S

+1.8V_DEEP_SUS
+VCCPGPPF R173 *0_6_S

+VCCDSW_1.0V C446 1U/6.3V_4
+1.0V_DEEP_SUS R434 *0_6_S +VCCMPHYAON_1P0, C253 1U/6.3V_4
+1.0V_DEEP_SUS C373 1U/6.3V_4, C491 47U/6.3V_8
+1.0V_DEEP_SUS R335 *0_6_S +VCCAMPHYPLL_1P0, C371 1U/6.3V_4
+1.0V_DEEP_SUS R334 *0_6_S +VCCAPLL_1.0V
+1.0V_DEEP_SUS R207 *0_6_S +VCCPRIM
+3VS5 R157 *0_4_S, C210 1U/6.3V_4, C170 0.1U/16V/X7R_4, C9752 *0.1P/50V_4
+V3.3DX_1.5DX_ADO L21 120/2000MA_6 +V3.3DX_1.5DX_ADO_R
+3V_DEEP_SUS R202 *0_6_S +VCCSPI
+1.0V_DEEP_SUS R201 *0_6_S +VCCSRAM_1.0V, C267 1U/6.3V_4
+3V_DEEP_SUS R90 *0_6_S +VCCPRIM_3.3V
+1.0V_DEEP_SUS R428 *0_6_S +VCCPRIM_1.0V
+1.0V_DEEP_SUS R330 *0_6_S +VCCAPLLEBB, C271 1U/6.3V_4

+V3.3DX_1.5DX_ADO R155 *0_4_S +3V
+1.0V_DEEP_SUS C372 *1U/6.3V_4, C375 *22U/6.3V_6
+3VS5 R308 *0_6_S, R126 *0_6_S +3V_DEEP_SUS

+VCCATS_1.8V C452 1U/6.3V_4
+VCCRTC C172 0.1U/16V/X7R_4, C165 1U/6.3V_4
+VCCRTCPRIM_3.3V C418 1U/6.3V_4, C425 0.1U/16V/X7R_4
+VCCPGPPB C431 *1U/6.3V_4
+VCCPGPPC C244 *1U/6.3V_4
+VCCPGPPE C256 1U/6.3V_4

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Custom	15 -- KABYLAKE 14/15(PCH POWER)	1A
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2,4,10,11,12,13,14,15,17,18,19,20,22,24,27,29,30,31,34,37,39,43,49 +3V
4,10,11,14,15 +3V_DEEP_SUS
9,13,15,48,49,52 +1.0V_DEEP_SUS
2,4,6,49,52 +VCCIO
4,10,12,15,19,21,23,25,27,28,31,32,36,37,42,48,49,50,52 +3VS5

EC-FVT-04

*Samtec BSH-030-01

CPU XDP

9	CFG3	R209 1K_4	30	GND16	GND(XDP_PRESENT#)	31	
12	XDP_PREQ#_CPU		29	XDP_TCK0	XDP_TMS	32	
12	XDP_PRDY#_CPU		28	XDP_TCK1	XDP_TDI	33	
9	CFG0	R232 1K_4	27	XDP_SCL	XDP_TRSTn	34	
9	CFG1		26	XDP_SDA	XDP_TDO	35	
9	CFG2		25	GND14	GND15	36	
	TP21	CFG3	24	HOOK3	HOOK7/DBR#	37	
2	XDP_BPM0		23	HOOK2	HOOK6/RESET#	38	
2	XDP_BPM1		22	VCC_OBS_AB	VCC_OBS_CD	39	
9	CFG4		21	HOOK1	ITPCLK#/HOOK5	40	
9	CFG5		20	HOOK0	ITPCLK/HOOK4	41	
9	CFG6		19	GND12	GND13	42	
9	CFG7		18	OBSDATA_B3	OBSDATA_D3	43	
4,29	RSMRST#	R203 1K_4	17	OBSDATA_B2	OBSDATA_D2	44	
4,29	DNBSWON#		16	GND10	GND11	45	
	+1.0V_DEEP_SUS		15	OBSDATA_B1	OBSDATA_D1	46	
	CFG0	R219 *0_4_S PWR_DEBUG	14	OBSDATA_B0	OBSDATA_D0	47	
		HOCK3	13	GND8	GND9	48	
10,17,18,31	SMB_RUN_DAT	R233 *0_4_S SMB_RUN_DAT_XDP	12	OBSFN_B1	OBSFN_D1	49	
10,17,18,31	SMB_RUN_CLK	R235 *0_4_S SMB_RUN_CLK_XDP	11	OBSFN_B0	OBSFN_D0	50	
		XDP_TCK1	10	GND6	GND7	51	
		XDP_TCK0	9	OBSDATA_A3	OBSDATA_C3	52	
2	XDP_TCK0		8	OBSDATA_A2	OBSDATA_C2	53	
			7	GND4	GND5	54	
			6	OBSDATA_A1	OBSDATA_C1	55	
			5	OBSDATA_A0	OBSDATA_C0	56	
			4	GND2	GND3	57	
			3	OBSFN_A1	OBSFN_C1	58	
			2	PROC_PREQ#	OBSFN_C0	59	
			1	XDP_PRESENT#	GND1	60	

CN3

CFG17 9
CFG16 9
CFG8 9
CFG9 9
CFG10 9
CFG11 9
CFG19 9
CFG18 9
CFG12 9
CFG13 9
CFG14 9
CFG15 9
CK_XDP_P 13
CK_XDP_N 13
+1.0V_DEEP_SUS
ITP_PMODE 9
SYS_RESET# 4,16
XDP_TDO
XDP_TRST#
XDP_TDI
XDP_TMS
TP23

HOCK3 R225 1K_4 +3V_DEEP_SUS

+3V *1K_4 R227 SYS_RESET#
C270 *0.1U/16V_4

+VCCIO
R220 150/F_4
PWR_DEBUG
R221 *10K_4

+1.0V_DEEP_SUS
C229 *0.1U/16V_4
C228 *0.1U/16V_4

APS

+3V_DEEP_SUS +3VS5

CN1

1	1		
2	2		
3	3		
4	4	SUSB#	4,29
5	5	SLP_S5#	4
6	6	SUSC#	4,29
7	7	SLP_A#	4,29
8	8		
9	9		
10	10	RTC_RST#	13
11	11	DNBSWON#	
12	12		
13	13	SYS_RESET#	4,16
14	14	PCH_SLP_S0_N	4
15	15		
16	16		
17	17		
18	18		

*50501-0180N-001

C463 *0.1U/16V_4

+3V R450 *0_4_S

4,29,47,50 HWPG

U30

	VCC	14			
XDP_TDO	1A	2	1B	3	XDP_TDO_CPU 2
	1OE	1			
XDP_TDI	2A	5	2B	6	XDP_TDI_CPU 2
	2OE	4			
XDP_TMS	3A	9	3B	8	XDP_TMS_CPU 2
	3OE	10			
XDP_TRST#	4A	12	4B	11	XDP_TRST#_CPU 2
	4OE	13			
	DPAD			15	
	GND			7	

*SN74CBTLV3126RGYR

2	JTAGX_PCH		XDP_TCK0
2	JTAG_TMS_PCH		XDP_TMS
2	JTAG_TDI_PCH		XDP_TDI
2	JTAG_TDO_PCH		XDP_TDO
2	JTAG_TCK_PCH		XDP_TCK1

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	16 -- KABYLAKE 15/15(XDP/APS)	1A
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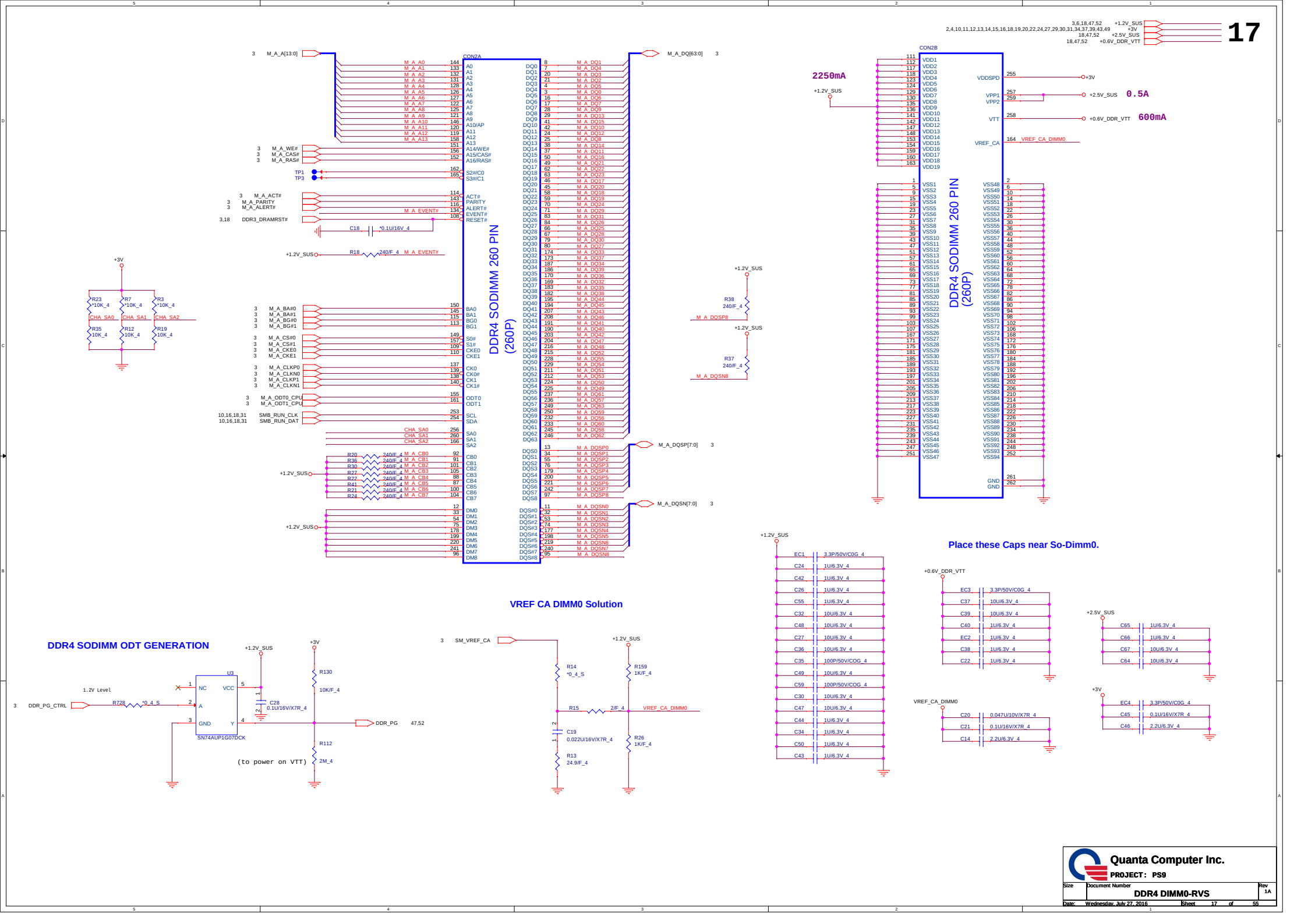
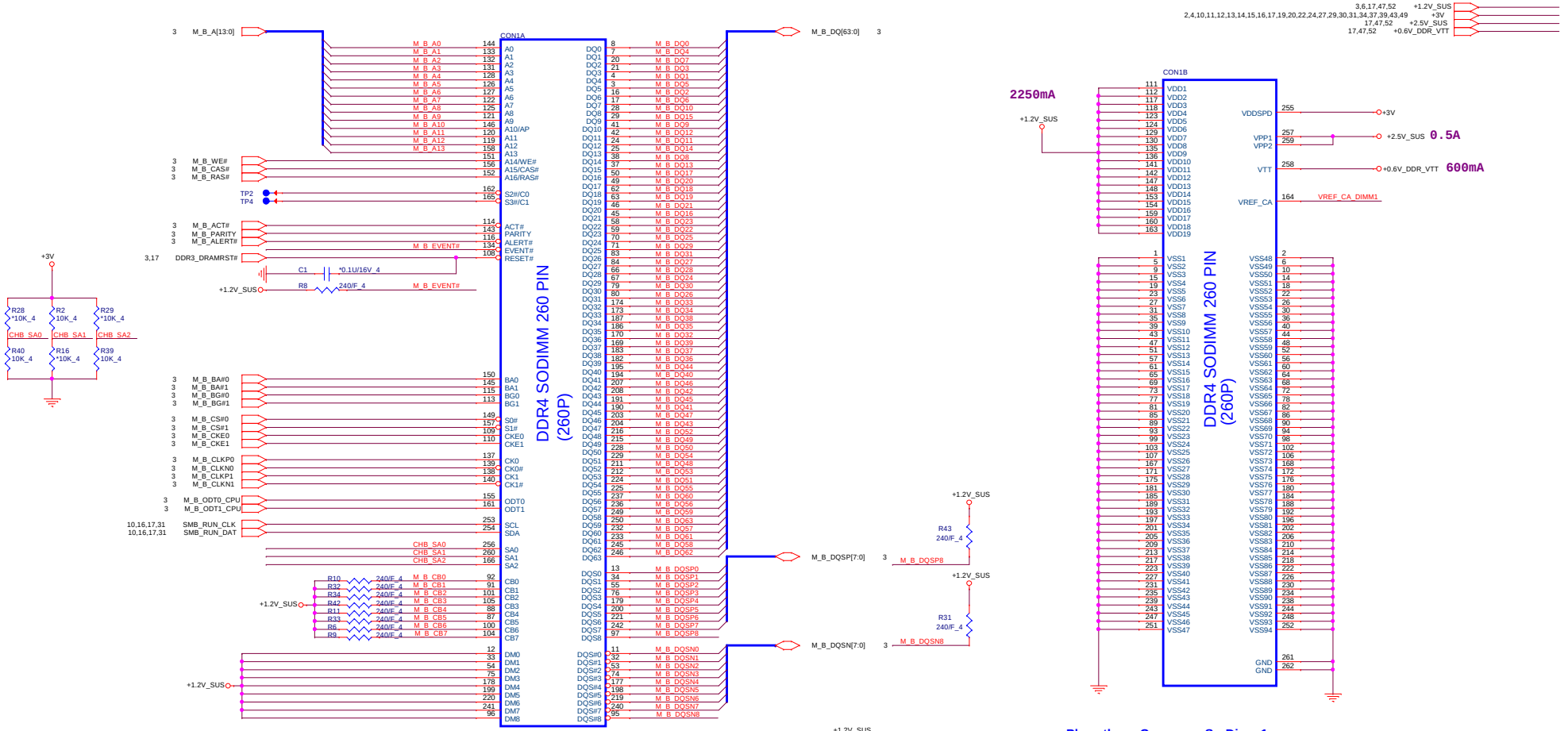
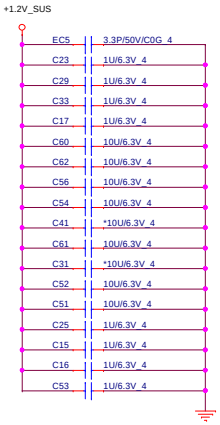
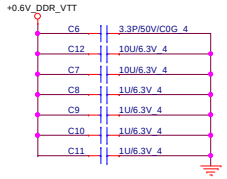
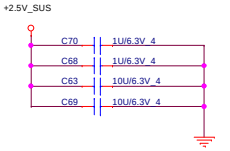

CON2A
DDR4 SODIMM 260 PIN (260P)
CON2B
DDR4 SODIMM 260 PIN (260P)
2250mA
0.5A
600mA
Place these Caps near So-Dimm0.
VREF CA DIMM0 Solution
DDR4 SODIMM ODT GENERATION
SN74AUP1G07DCK
(to power on VTT)
Quanta Computer Inc.
PROJECT: PS9
DDR4 DIMM0-RVS
Wednesday, July 27, 2016

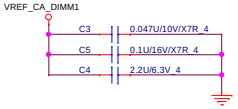


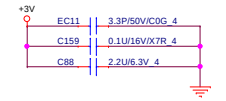
Place these Caps near So-Dimm1



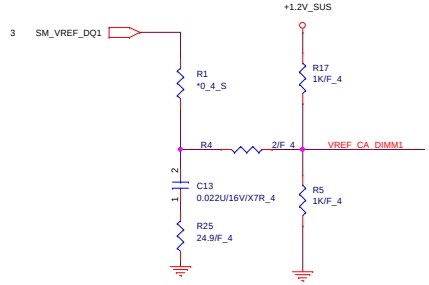








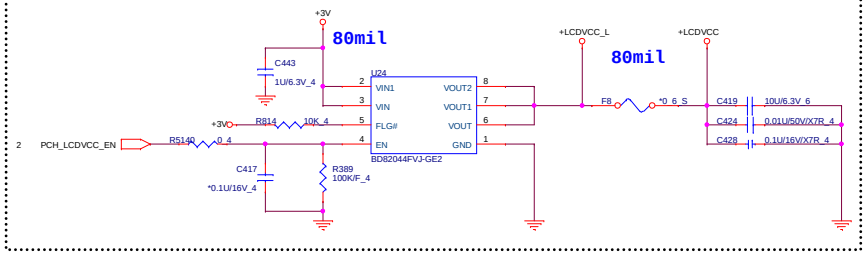
VREF CA DIMM1 Solution



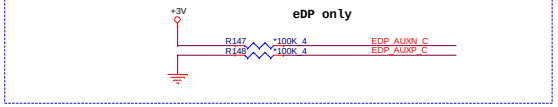
Quanta Computer Inc.			
PROJECT: PS9			
Size	Document Number		Rev
	DDR4 DIMM1-RVS		1A
Date: Wednesday, July 27, 2016	Sheet 18 of 55		

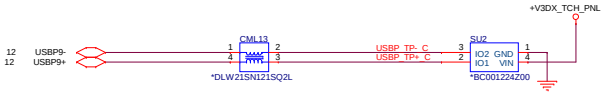
13,22,25,29,32,33,37,41,42,53 +3VPCU
2,4,10,11,12,13,14,15,16,17,18,20,22,24,27,29,30,31,34,37,39,43,49 +3V
41,42,43,44,45,46,47,48,51,52 +VIN
22 +V3.3DX_AUDIO
4,10,12,15,16,21,23,25,27,28,31,32,36,37,42,48,49,50,52 +3VS5
4,26,27,28,32,33,37,42,43,46,47,48,49,50,52 +5VS5

LCDVCC

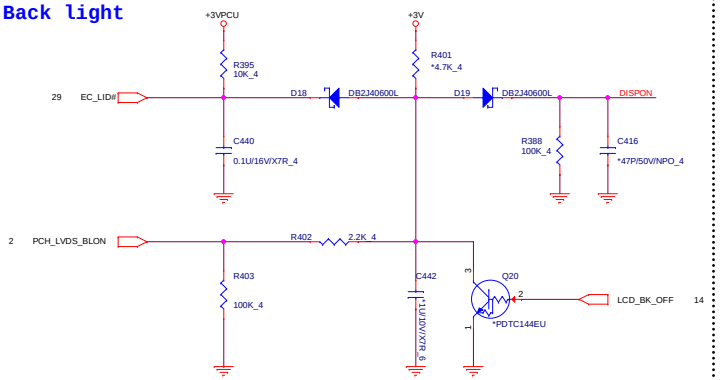


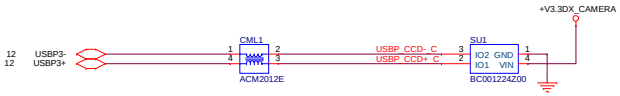
eDP only



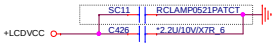


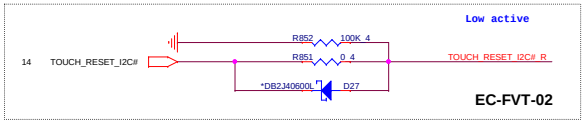
Back light



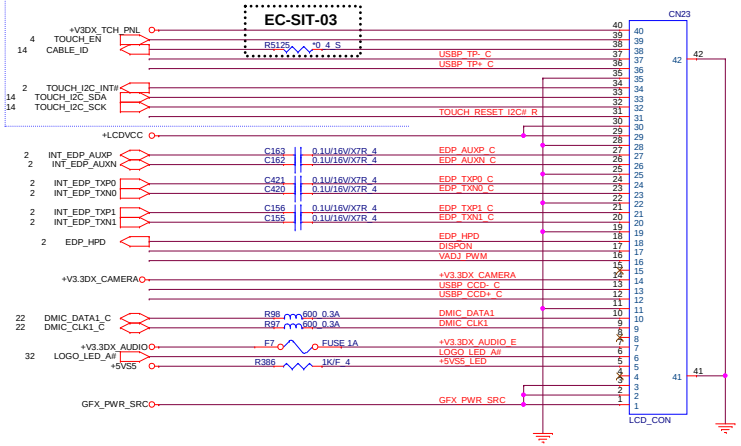


For ESD

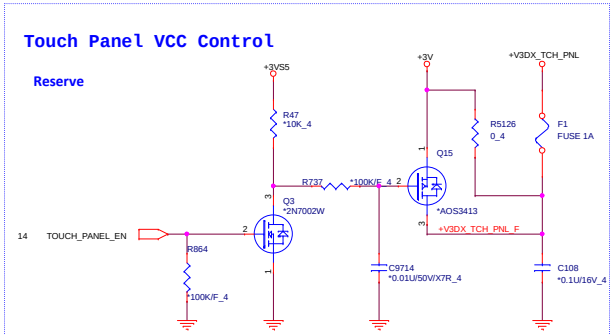




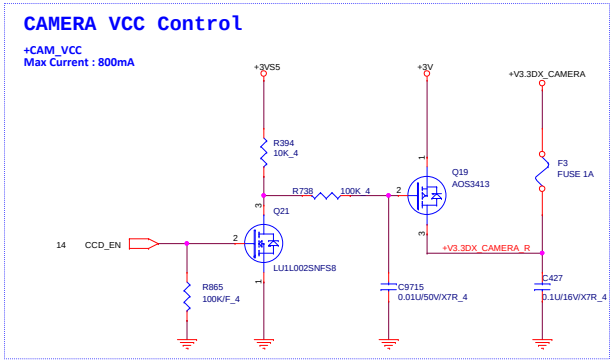
Touch Panel



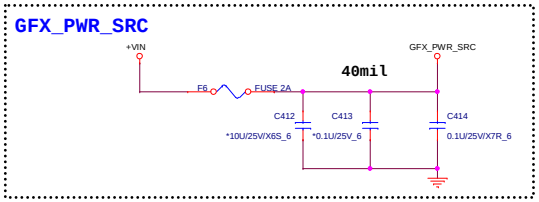
Touch Panel VCC Control

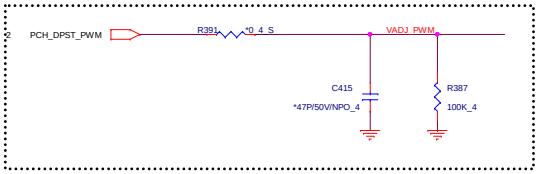


CAMERA VCC Control



GFX_PWR_SRC





Quanta Computer Inc.
PROJECT: PS9
Size
Document Number
LCD/CAMERA/Touch Panel/MIC
Rev
1A
Date: Wednesday, July 27, 2016
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2,4,10,11,12,13,14,15,16,17,18,19,22,24,27,29,30,31,34,37,39,43,49 +3V
22,30,31,33,49 +5V
50,52 +1.5V

U7
PS8407ATQFN40GTR2-A1

EMI reserve for HDMI

HDMI HPD SENSE

U4 U8 U26
ESD8004MUTAG

For ESD

Layout note:Place close to HDMI Conn

CN9
HDMI CONN

Quanta Computer Inc.			
PROJECT: PS9			
Size	Document Number		Rev
	HDMI CONN		1A
Date: Wednesday, July 27, 2016	Sheet 20	of	55

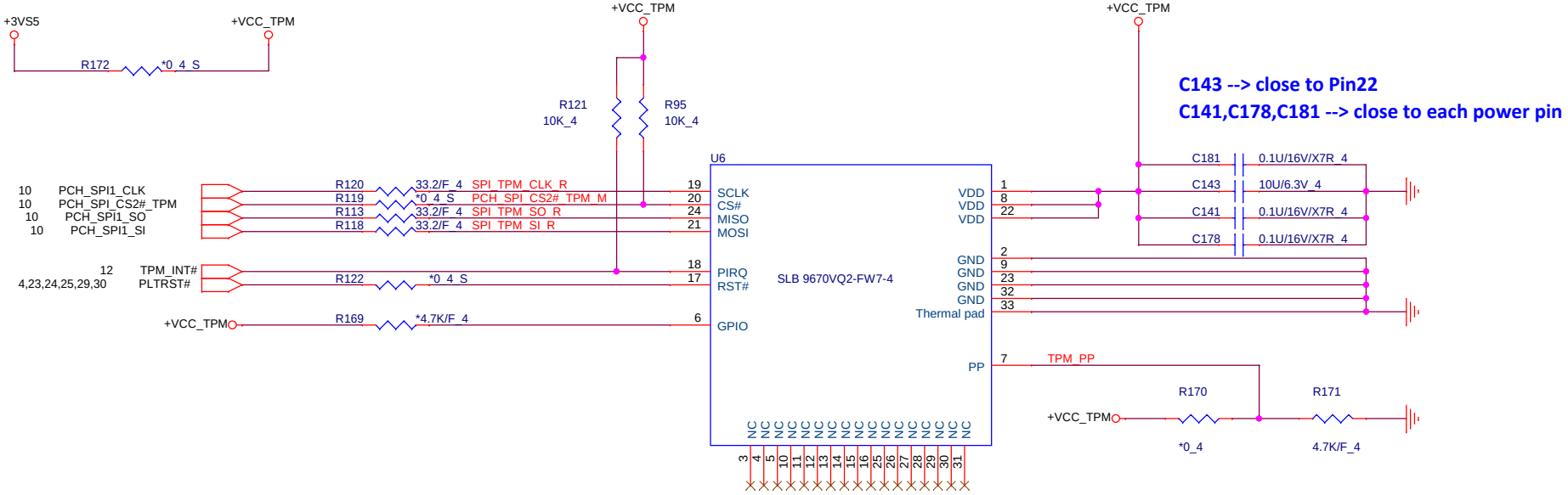
TPM

AL33HTPH001:ST33HTPH2E32AHA6

2,4,10,11,12,13,14,15,16,17,18,19,20,22,24,27,29,30,31,34,37,39,43,49
4,10,12,15,16,19,23,25,27,28,31,32,36,37,42,48,49,50,52

+3V
+3VS5

21



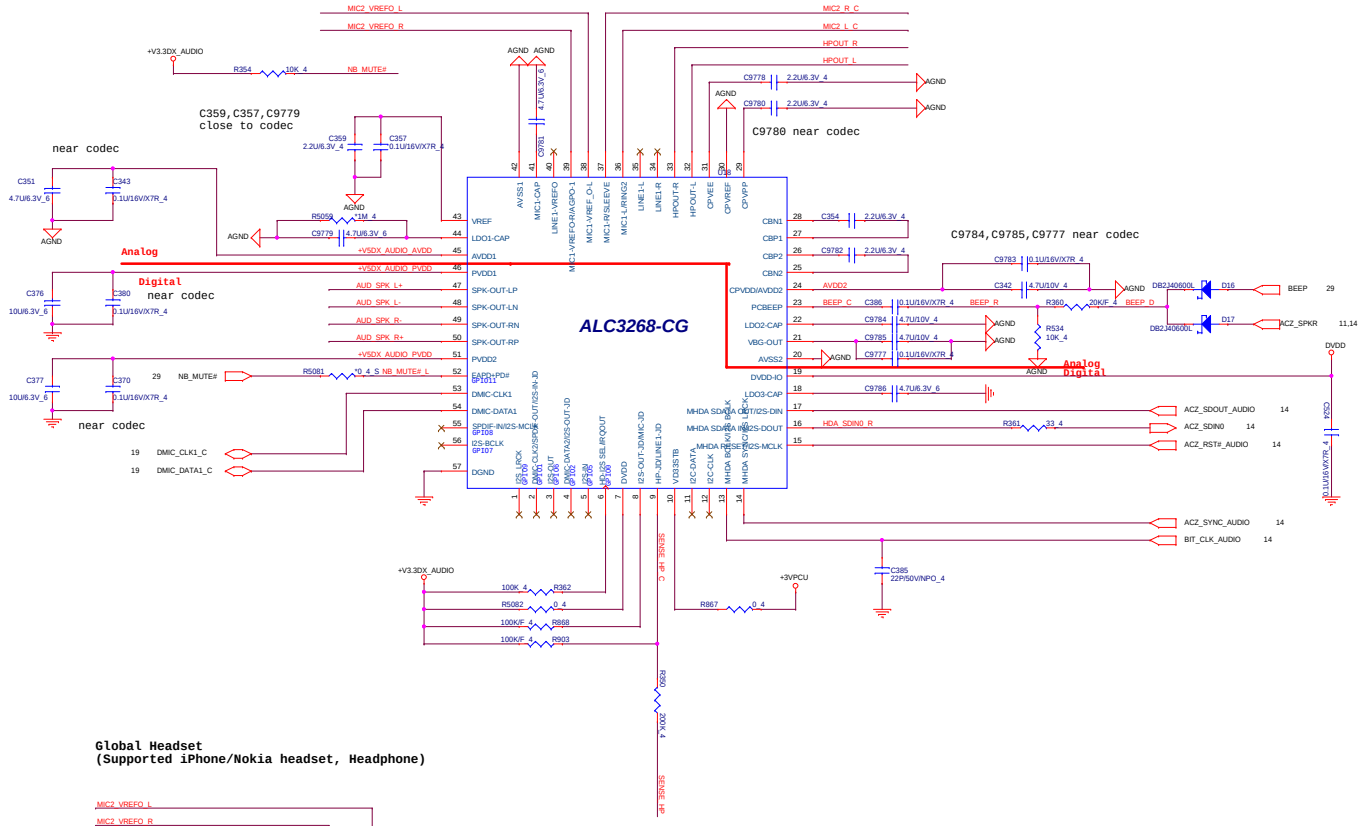
C143 --> close to Pin22
C141,C178,C181 --> close to each power pin

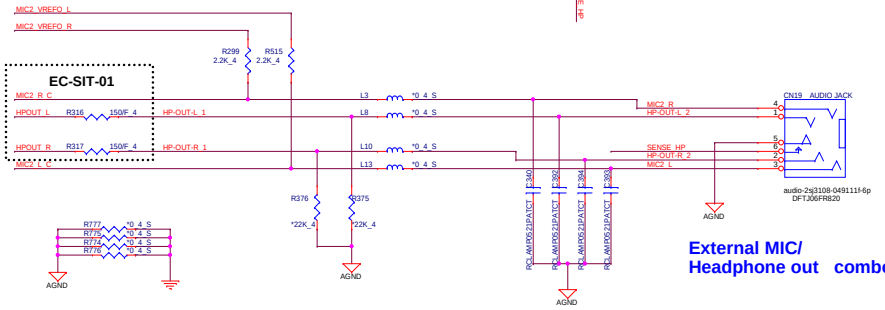
EC-SIT-07

Quanta Computer Inc.
PROJECT: PS9

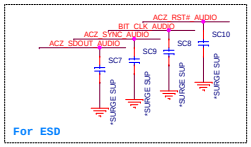
Size	Document Number	Rev
	TPM/RFID	1A
Date: Wednesday, July 27, 2016	Sheet 21 of 55	

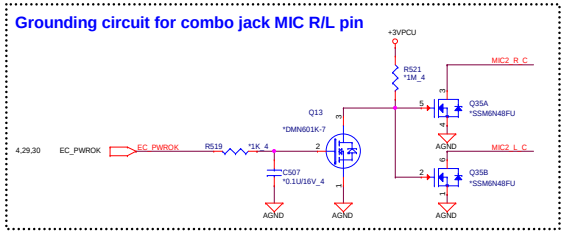
ALC3268

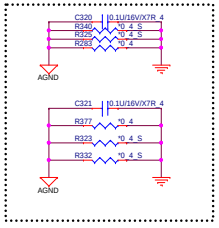


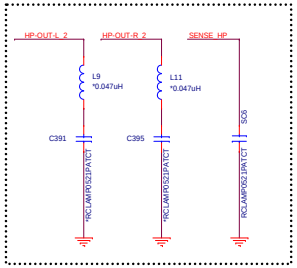


External MIC/
Headphone out combo

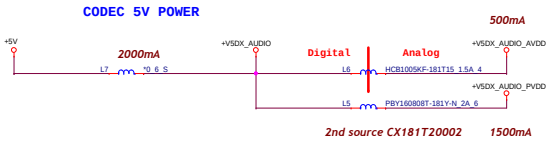


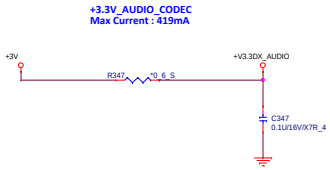


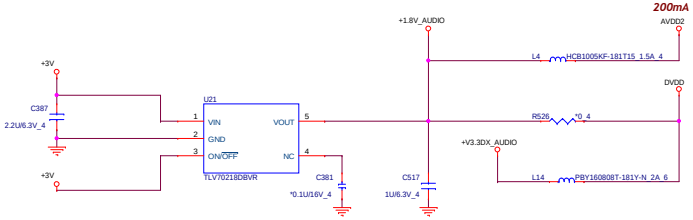




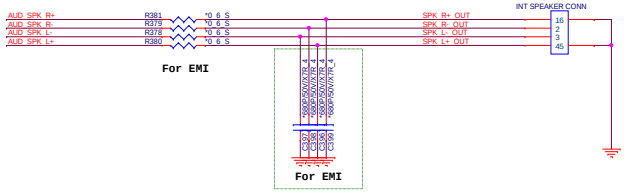
22







INT Speaker



Quanta Computer Inc.			
PROJECT: PS9			
Size	Document Number		Rev
	Audio(ALC3268)		1A
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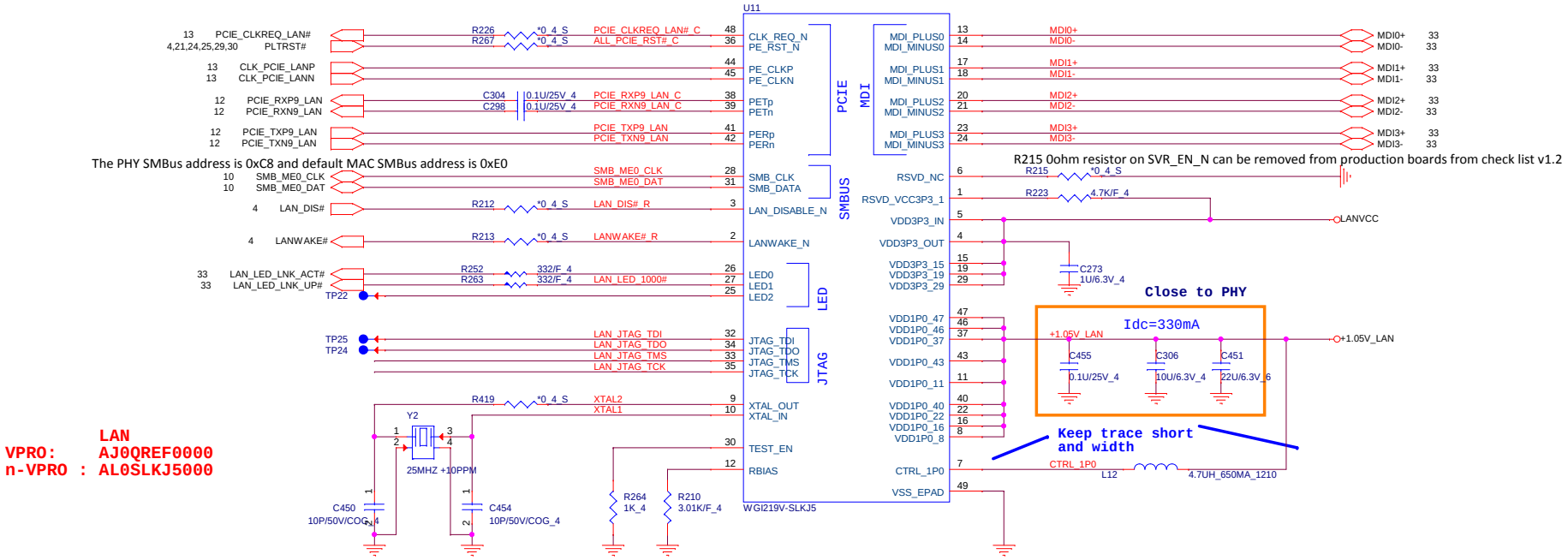
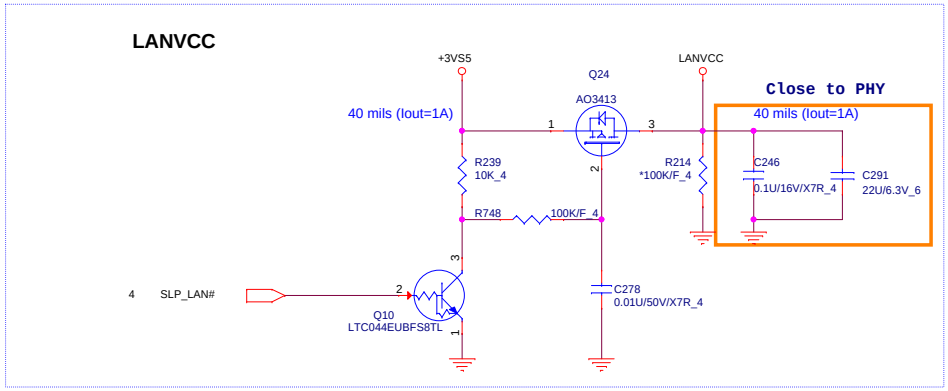
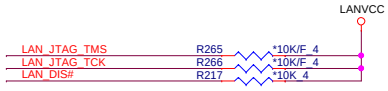
4,10,12,15,16,19,21,25,27,28,31,32,36,37,42,48,49,50,52 +3VS5



LAN
VPRO: AJ0QREF0000
n-VPRO : AL0SLKJ5000



LANVCC
Trace width>60mil,
Trace length<200mil



Quanta Computer Inc.
PROJECT: PS9

Size	Document Number	Rev
	LAN Intel I219LM	1A
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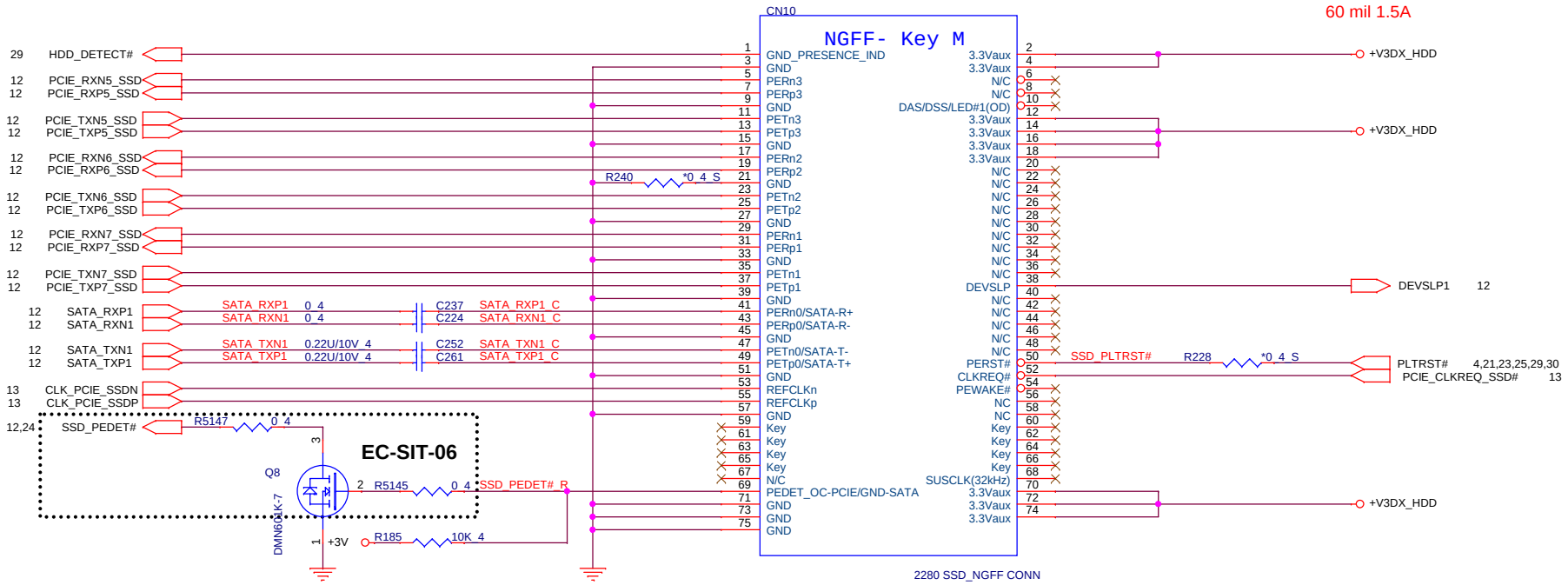
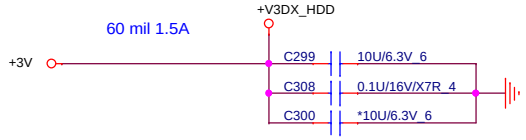
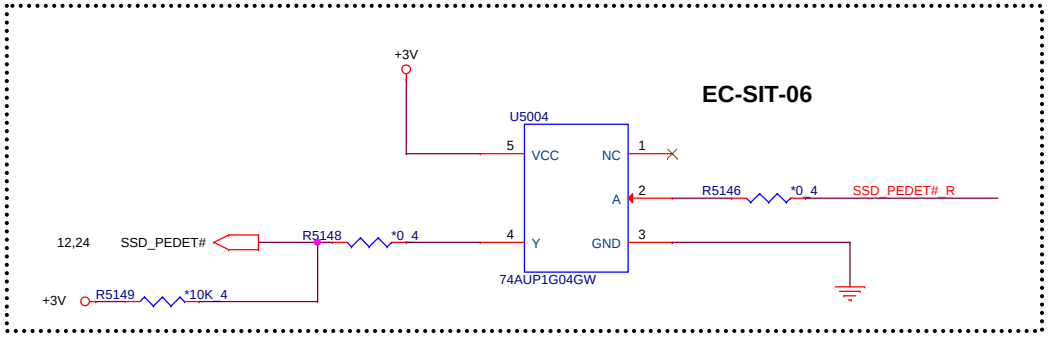
SSD M.2

2,4,10,11,12,13,14,15,16,17,18,19,20,22,27,29,30,31,34,37,39,43,49 +3V



DC Current rating: 3 A (MAX)





Quanta Computer Inc.		
PROJECT: PS9		
Size	Document Number: SATA/PCIE SSD M.2	Rev: 1A
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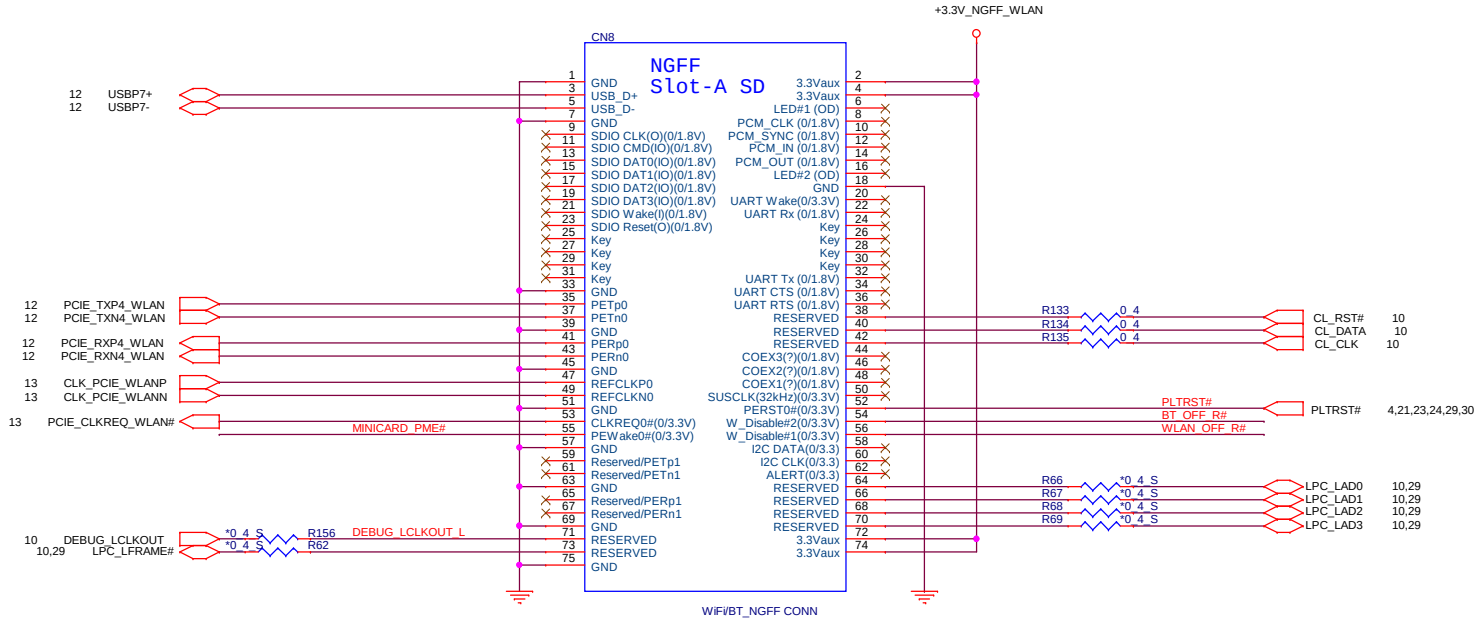
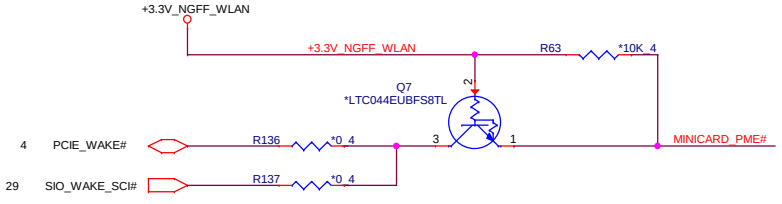
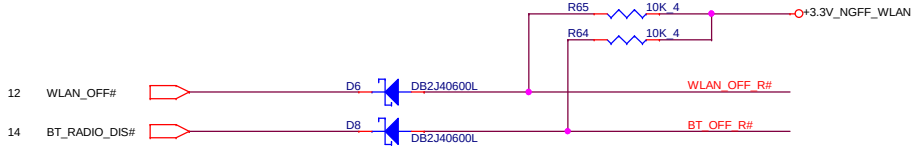
NGFF WiFi/BT connector
M.2 2230

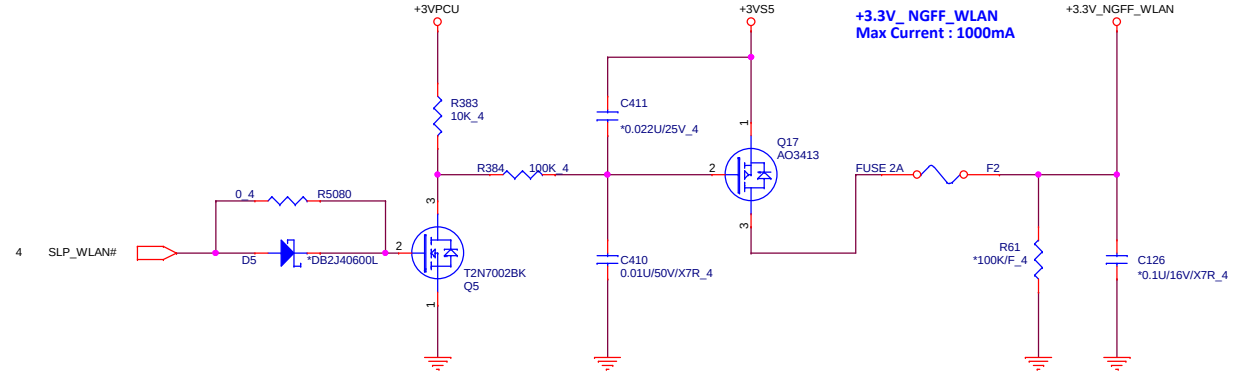
25

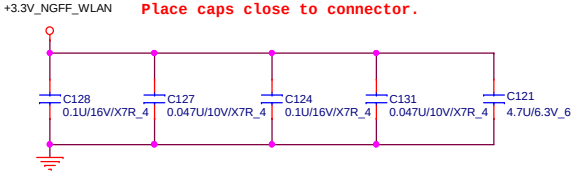
4,10,12,15,16,19,21,23,27,28,31,32,36,37,42,48,49,50,52 +3VS5
13,19,22,29,32,33,37,41,42,53 +3VPCU











Quanta Computer Inc.
PROJECT: PS9

Size	Document Number	Rev
	Wifi/BT NGFF	1A
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The SMBus slave address of RTS5412 is default set to be 1101010b

4,19,27,28,32,33,37,42,43,46,47,48,49,50,52 +5VS5

+5VS5 +5VS5HUB R543 *0_6_S

+5VS5HUB R544 4.7K_4 HUB_BPWR_DET R545 10K_4

+3V_HUB R546 10K_4 HUB_SPWR_DET

Q46 SSM6N48FU

HUBGPIO1 MBDATA_THRM 10,29,30

HUBGPIO0 MBCLK_THRM 10,29,30

Close to U37

C543 18P/50V/COG_4 HUB_XTLO

Y4 12MHZ +20PPM

C544 18P/50V/COG_4 HUB_XTLI

+3V_HUB R788 10K_4 OCP3 R789 10K_4 OCP4

+5VS5 R557 100K_4 R558 100K_4 DP1_PWR DP2_PWR R559 200K_4 R560 200K_4

3.3V output

5V to 3.3V LDO input

U52B_RTS5411-GR

AV12_1 AV12_2 AV12_3 AV12_4 AV12_5 AV12_6 AV12_7 AV12_8 DV12_1

AV33HP0 HUBOUT_3V3 R811 *0_6_S

V33_OUT V5_IN_HUB R813 *0_6_S

V5_IN V5_SWR_HUB R812 *0_6_S

V5_IN_SWR DV12_2_LX L20 4.7UH_760MA

SWR_OUT

Gang_UpGND R803 *0_4_S

HG5V_SWR DV12_2

DV12/VO12/VO15 DV12_3

E_PAD

+3V_HUB +5VS5HUB +1.2V_HUB

+3V_HUB R659 10K_4 HUB_SPI_CS_N

Vender	Size	P/N
MX	128KB	AKE35FN0Z03 (MX25V1035FM1I)
Winbond	128KB	AKE35ZN0N00 (W25X10CLSNIG)

HUB_SPI_CS_N R655 *0_4_S HUB_SPI_CS_N_C

HUB_SPI_SCK R656 *0_4_S HUB_SPI_SCK_C

HUB_SPI_MOSI HUB_SPI_MISO

U45 W25X10CLSNIG CE# SCK SI SO WP# VDD HOLD# VSS

+3V_HUB R658 10K/F_4 R657 10K/F_4 C615 0.1U/16V/X7R_4

U52A_RTS5411-GR

HUB_SPI_MISO HUB_SPI_MOSI HUB_SPI_SCK HUB_SPI_CS_N MISO MOSI SCK SCS

HUB_XTLI HUB_XTLO XTLI XTLO

R792 6.2K/F_4 HUB_RREF RREF

HUB_SPWR_DET SPWR_DET

29 HUB_BPWR_DET BPWR_DET

27 USBHUB_OC1# 27 USBHUB_OC2# OCP3 OCP4 OCP1 OCP2 OCP3 OCP4

27 DP1_PWR 27 DP2_PWR TP50 DP1_PWR DP2_PWR DP3_PWR DSP1_PWR DSP2_PWR DSP3_PWR DSP4_PWR

R551 R552 R553 R554 R810 R809 R808 R807 10K_4 *4.7K_4 HUBGPIO0 HUBGPIO1 HUBGPIO2 HUBGPIO3 HUBGPIO4 HUBGPIO5 HUBGPIO6 HUBGPIO7 GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7

USP_DP USP_DM USP_SSRX+ USP_SSRX- USP_SSTX+ USP_SSTX- DSP1_DP DSP1_DM DSP1_SSRX+ DSP1_SSRX- DSP1_SSTX+ DSP1_SSTX- DSP2_DP DSP2_DM DSP2_SSRX+ DSP2_SSRX- DSP2_SSTX+ DSP2_SSTX- DSP3_DP DSP3_DM DSP3_SSRX+ DSP3_SSRX- DSP3_SSTX+ DSP3_SSTX- DSP4_DP DSP4_DM DSP4_SSRX+ DSP4_SSRX- DSP4_SSTX+ DSP4_SSTX-

USB30_TX3+ USB30_TX3- USB30_RX3+_HUB C536 USB30_RX3-_HUB C537

0.1U/16V/X7R_4 USB30_RX3+ 0.1U/16V/X7R_4 USB30_RX3-

USBP2+ USBP2- USB30_TX3+ USB30_TX3- USB30_RX3+ USB30_RX3- DSP1_DP DSP1_DM DSP1_SSRX+ DSP1_SSRX- DSP1_SSTX+ DSP1_SSTX- DSP2_DP DSP2_DM DSP2_SSRX+ DSP2_SSRX- DSP2_SSTX+ DSP2_SSTX- USBP4+ USBP4-

FROM SOC

Cardreader

Close to U37.4/14/35/53

0.1U/16V/X7R_4 C545 C547 C549 C551

Close to each pin

0.1U/16V/X7R_4 C546 AV12_1 C548 AV12_2 C550 AV12_3 C552 AV12_4 C553 AV12_5 C554 AV12_6 C555 AV12_7 C556 DV12_1 C557 AV12_8 C9749 DV12_2 C9750 DV12_3

V5_SWR_HUB C531 0.1U/16V/X7R_4 C530 10U/6.3V_4

Close to pin 52

+1.2V_HUB C540 10U/6.3V_4

V5_IN_HUB C535 0.1U/16V/X7R_4 C534 10U/6.3V_4

HUBOUT_3V3 C533 0.1U/16V/X7R_4 C532 4.7U/6.3V_4

Quanta Computer Inc.

PROJECT: PS9

Size	Document Number	Rev
Custom	USB HUB-RTS5411	1A

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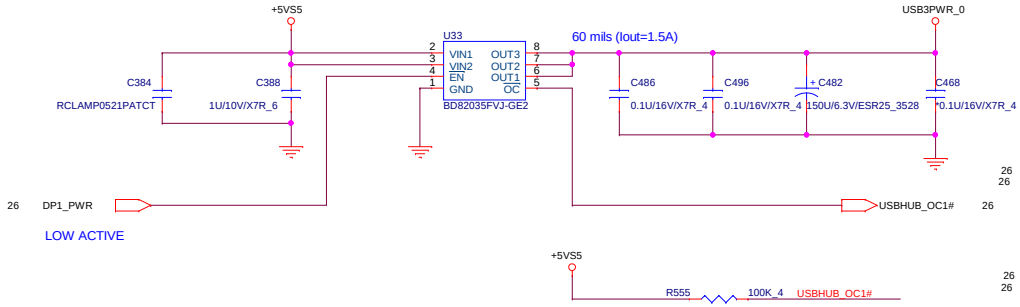
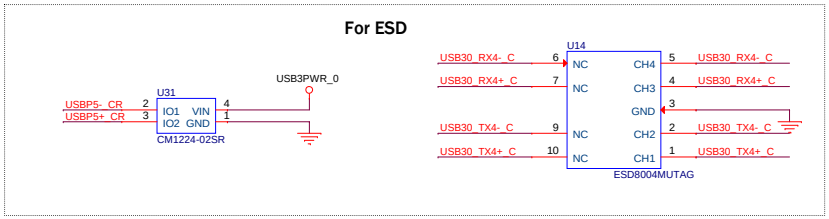
USB 3.0 Port L-side





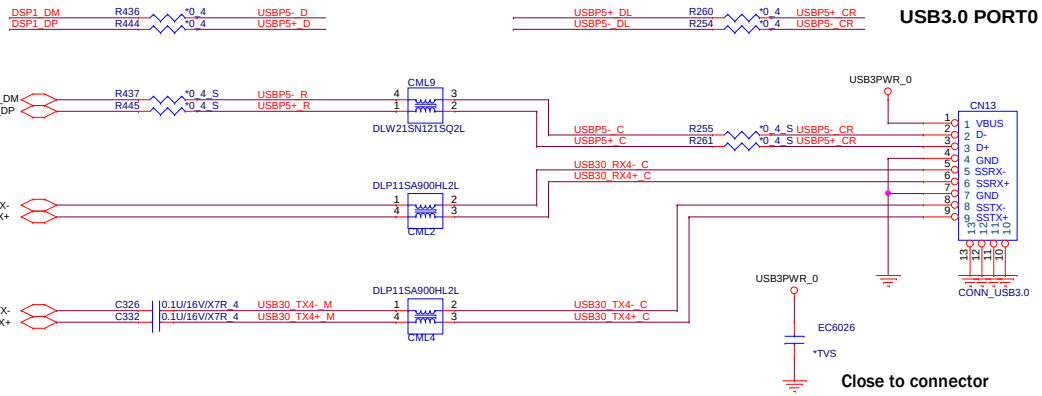
4,19,26,28,32,33,37,42,43,46,47,48,49,50,52
2,4,10,11,12,13,14,15,16,17,18,19,20,22,24,29,30,31,34,37,39,43,49
+5VS5
+3V

3 pad design

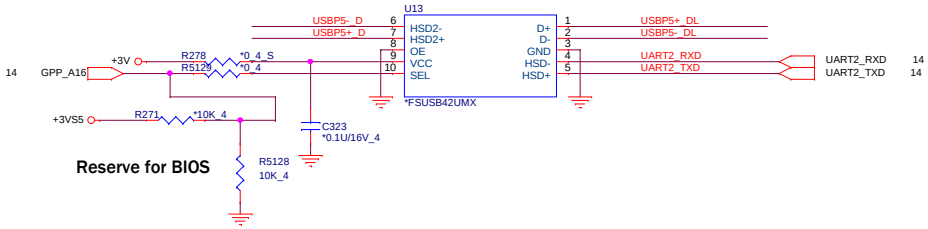
3 pad design

27

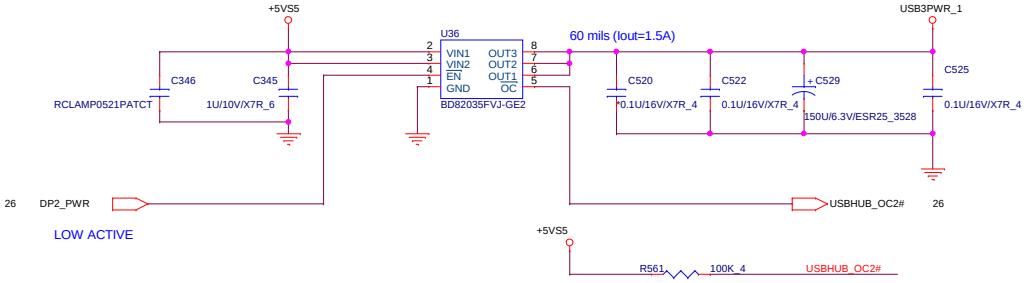
USB3.0 PORT0

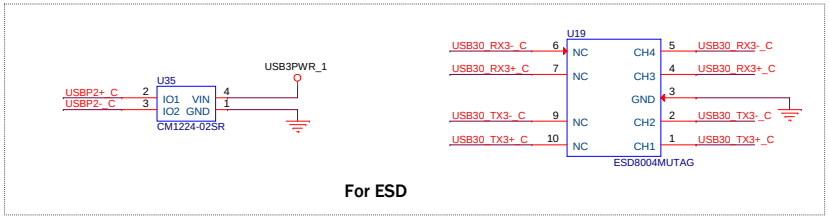


UART for DEBUG

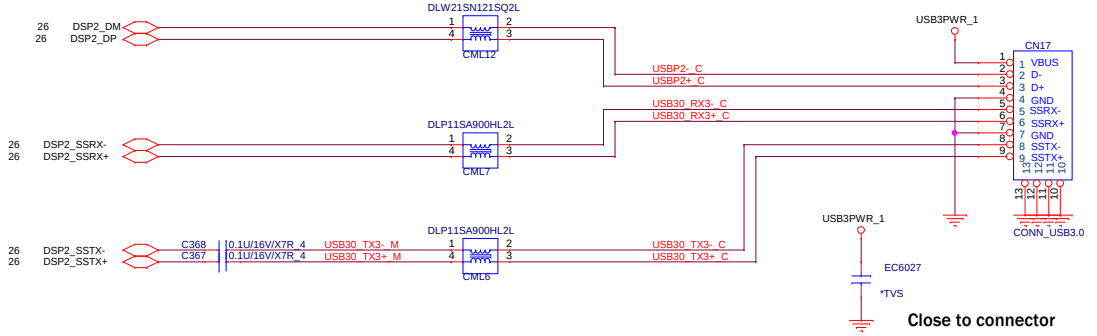


USB 3.0 Port R-side





USB3.0 PORT1



Quanta Computer Inc.

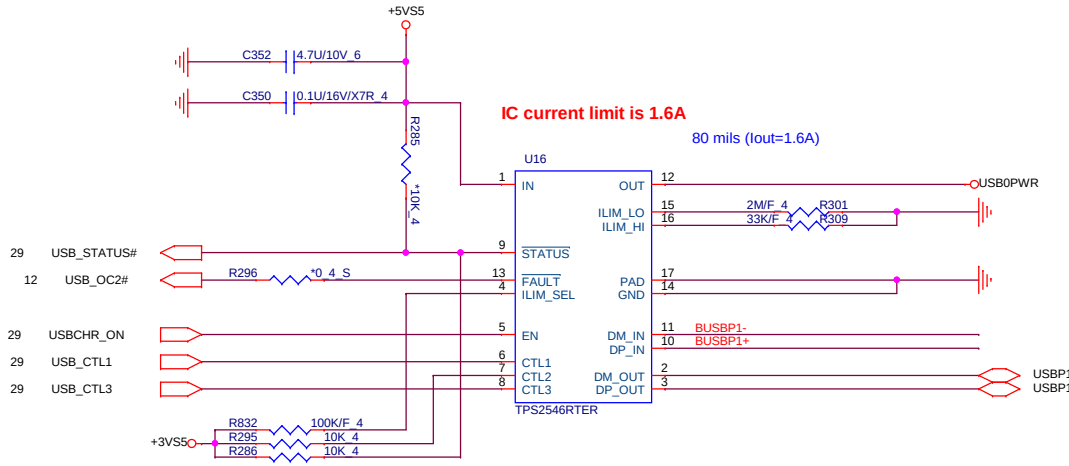
PROJECT: PS9

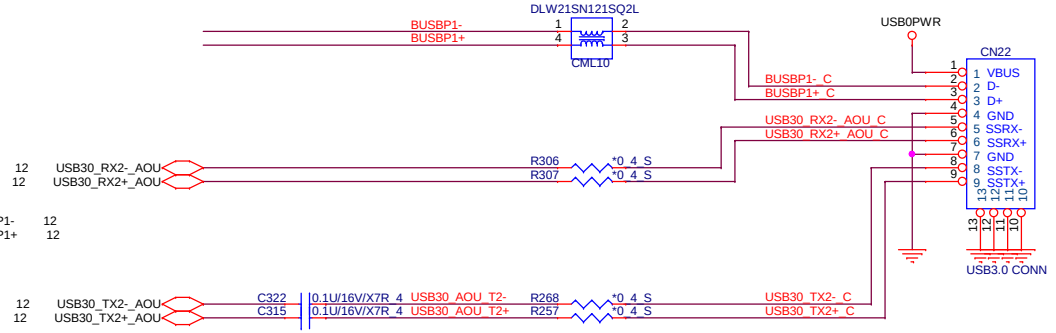
Size	Document Number	Rev
	USB3.0 X2	1A
Date: Wednesday, July 27, 2016	Sheet 27 of 55	

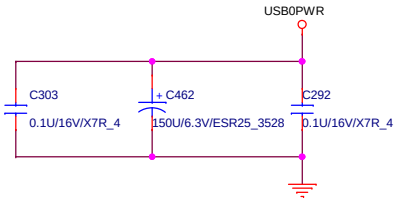
USB 3.0 Port (AOU5)

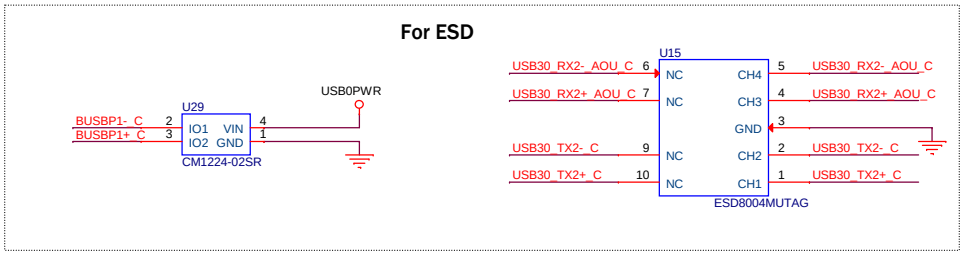
4,19,26,27,32,33,37,42,43,46,47,48,49,50,52
4,10,12,15,16,19,21,23,25,27,31,32,36,37,42,48,49,50,52
+5VS5
+3VS5

28









Quanta Computer Inc.		
PROJECT: PS9		
Size	Document Number	Rev
	UB3(AOU5)	1A
Date: Wednesday, July 27, 2016	Sheet 28 of 55	

ITE8886H

FOR EC auto load code

EC-FVT-09

For EMI, Close EC. pin74

Layout Note:
Place all capacitors close to IT8512.

EMI suggestion:
Add a 15p bypass
CAP on CLK_PCI_8512

For ESD

For PLL Power

For ESD

For ESD

LPC

GPIO

SM BUS

PS/2

HSPI

CIR

PWM

FSPI

EXTERNAL SERIAL FLASH

SPI ENABLE

A/D D/A

KBMX

CLOCK

Auto Load Code
Close to EEPROM

SPI NOR FLASH

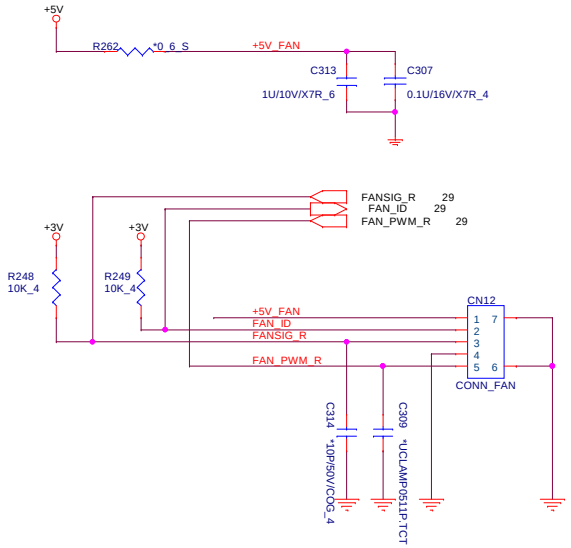
Thermal reset function

POWER SWITCH

Quanta Computer Inc.
PROJECT: PS9

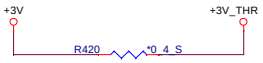
Size	Document Number	Rev
Custom	KBC IT8886	1A
Date: Wednesday, July 27, 2016	Sheet 29 of 55	

FAN CONN



Thermal Sensor

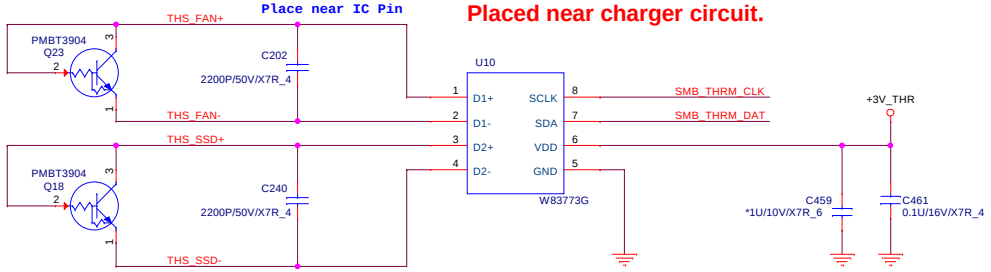
2,4,10,11,12,13,14,15,16,17,18,19,20,22,24,27,29,31,34,37,39,43,49 +3V
20,22,31,33,49 +5V



Placed near FAN

NOTE:
Place near IC Pin

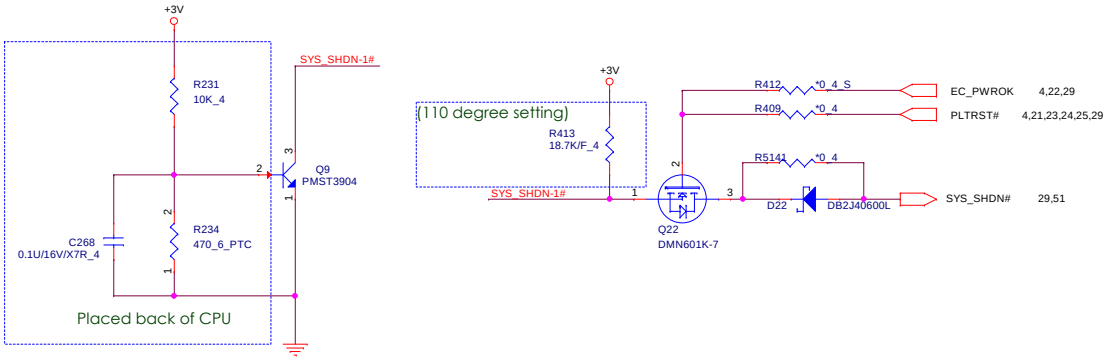
Placed near charger circuit.

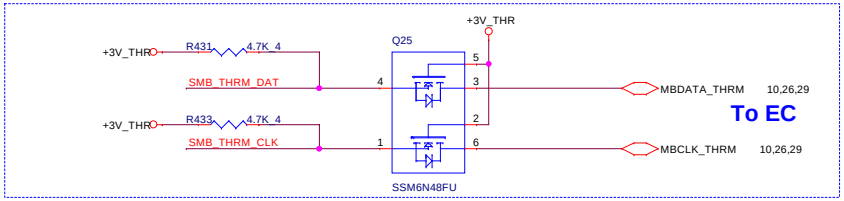


Placed near SSD

ADDRESS: 98H

CPU PTC circuit





Quanta Computer Inc.
PROJECT: PS9

Size	Document Number	Rev
	FAN/Thermal	1A
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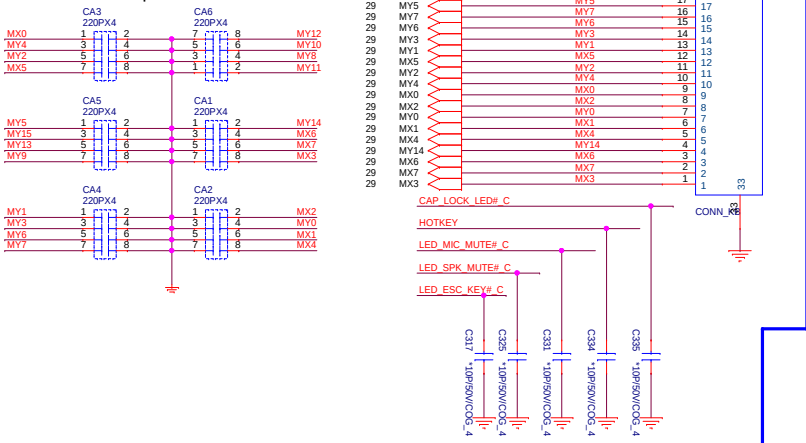
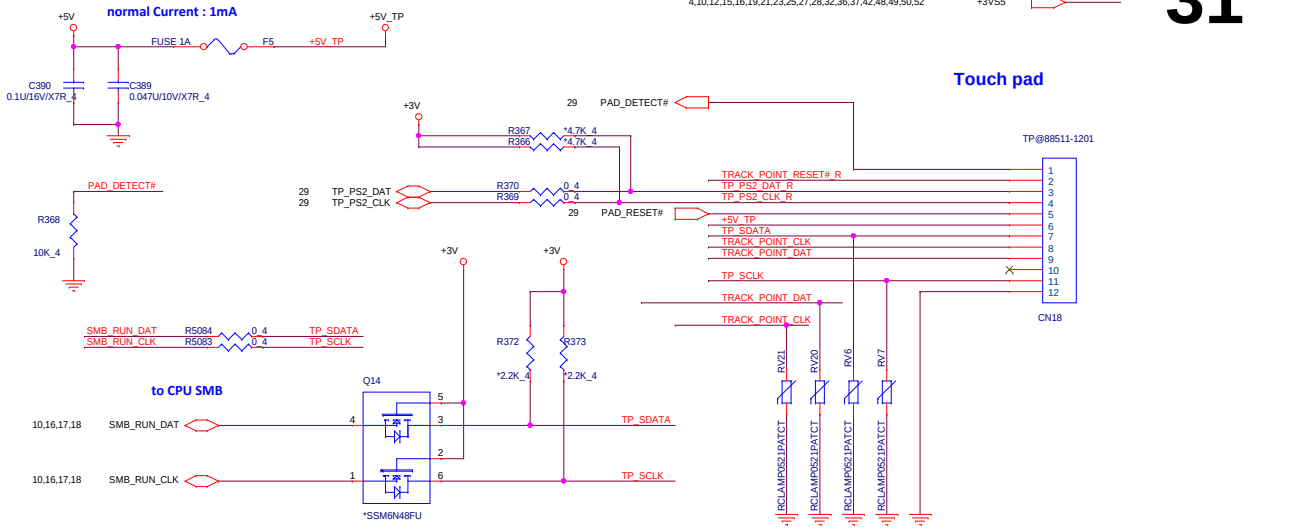
KEYBOARD

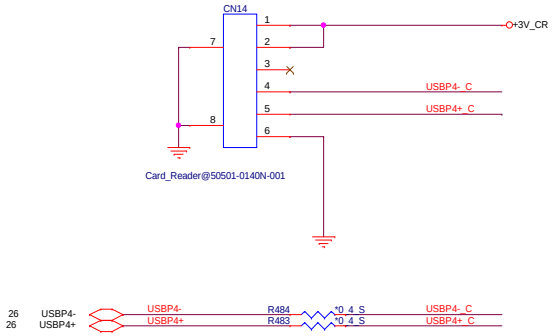
For EMI request



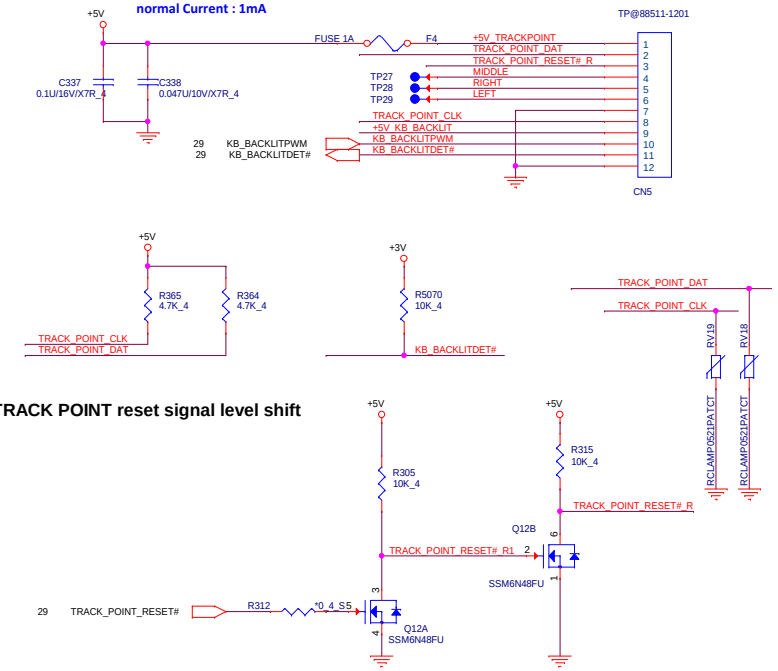
TP Control



To Card Reader Board

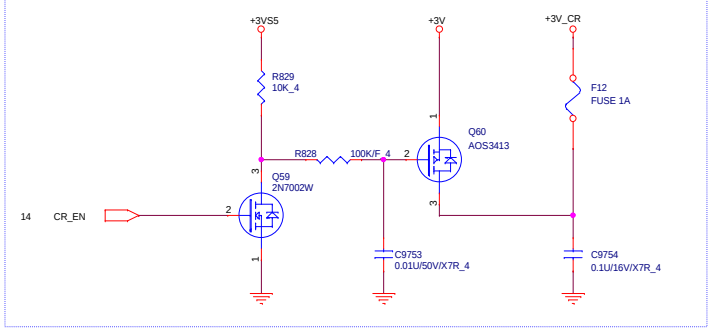


Track point

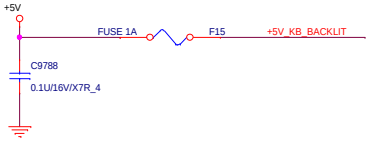


TRACK POINT reset signal level shift

CR VCC Control



KB backlit



Quanta Computer Inc.
PROJECT: PS9
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4,19,26,27,28,33,37,42,43,46,47,48,49,50,52 +5VS5
13,19,22,25,29,33,37,41,42,53 +3VPCU
4,10,12,15,16,19,21,23,25,27,28,31,36,37,42,48,49,50,52 +3VS5

Power Switch

29,33,37 NBSWON# NBSWON# SW1 TME-533B-Q-T/R RV1 RCLAMP0521PATCT

LID Switch

+3VPCU APX8132HAI-TRG S VDD GND N OUT LID# LID# 29 U1 C2 1U/6.3V_4

LED Driver

+3VS5 R452 100K_4 R461 *100K/J_4 29 LOGO_LED# Q29 SSM6N48FU
+5VS5 R460 10K_4 R492 *0_4_S Q32 LU1L002SNFS8 LOGO_LED_C# SC13 RCLAMP0521PATCT LED_CON CN15 R503 1K/F_4 +5VS5
LOGO_LED_A# 19

to C cover logo LED

Physical Reset BTN

+3VPCU R304 1K/F_4 SW2 TME-533B-Q-T/R R297 10K_4 BAT_EN_SW PD2034 DA2J10100L BAT_EN 41 C9751 1U/6.3V_4 R704 1K/F_4 Q11 SSM6N48FU R302 *0_4 EC_PWR_OFF_1# 41,42 EC_PWR_OFF_2# 42

14 LED_MIC_MUTE
14 LED_SPK_MUTE
Q28 R457 100K_4 R456 100K_4 R282 560_4 R269 560_4 SSM6N48FU
LED_MIC_MUTE#_C 31
LED_SPK_MUTE#_C 31

14 LED_ESC_KEY
14 CAP_LOCK_LED
Q31 R455 100K_4 R481 100K_4 R256 100_4 R288 100_4 SSM6N48FU
LED_ESC_KEY#_C 31
CAP_LOCK_LED#_C 31

29 BATLED_GREEN_LED_EC
29 BATLED_AMBER_LED_EC
Q2 R57 100K_4 R51 100K_4 SSM6N48FU
BATLED_GREEN_LED#
BATLED_AMBER_LED#

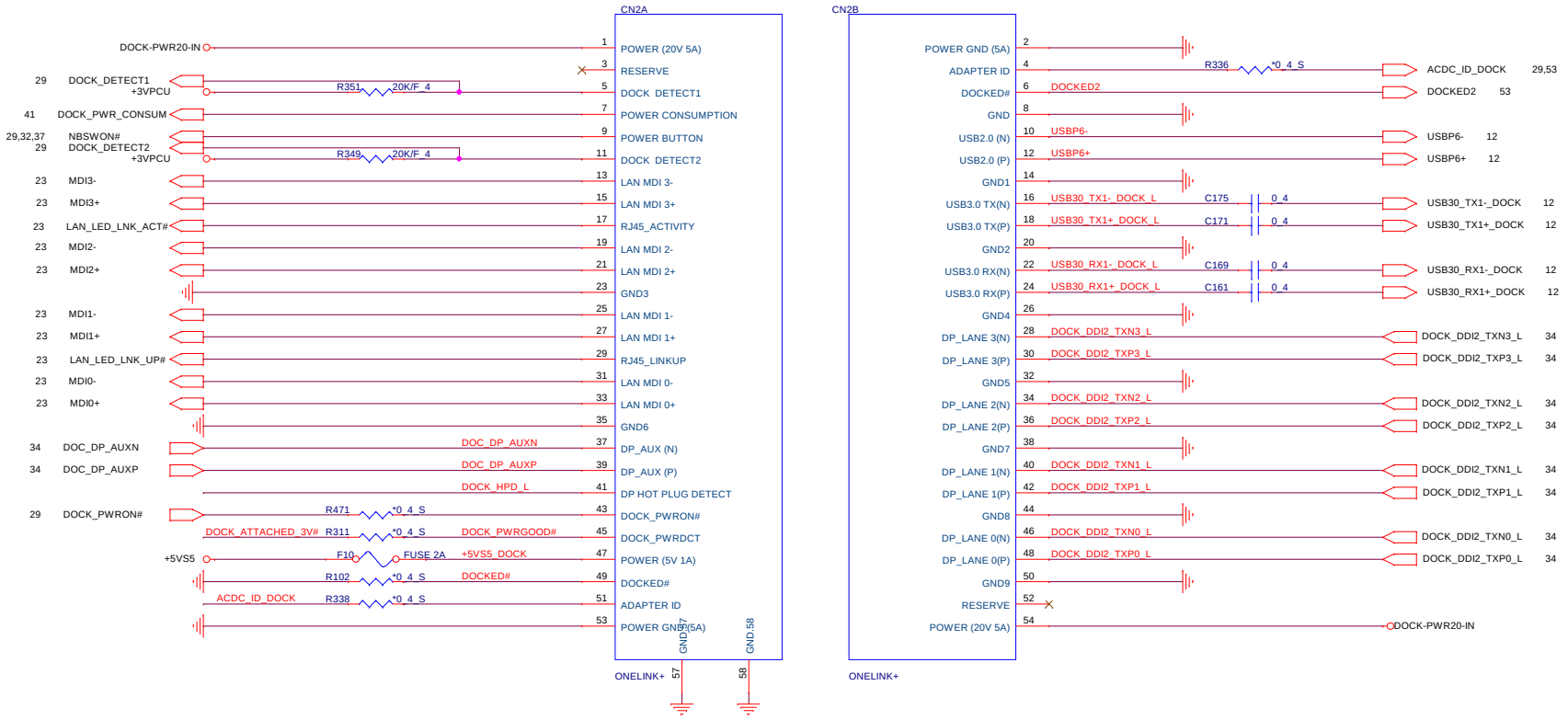
BATLED_GREEN_LED# R46 82.5/F_6 BATLED_GREEN_LED#_R
BATLED_AMBER_LED# R50 210/F_4 BATLED_AMBER_LED#_R
LED1 GREEN ORANGE GREEN/ORANG-LED +3VS5
RCLAMP0521PATCT C103 RCLAMP0521PATCT C401

Battery

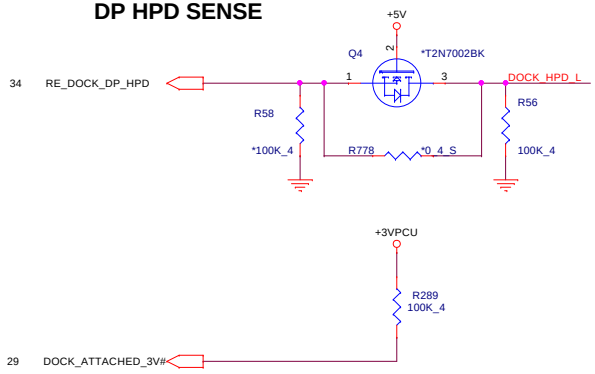
Quanta Computer Inc.			
PROJECT: PS9			
Size: Custom	Document Number: LED/SW	Rev: 1A	
Date: Wednesday, July 27, 2016	Sheet: 32	of: 55	

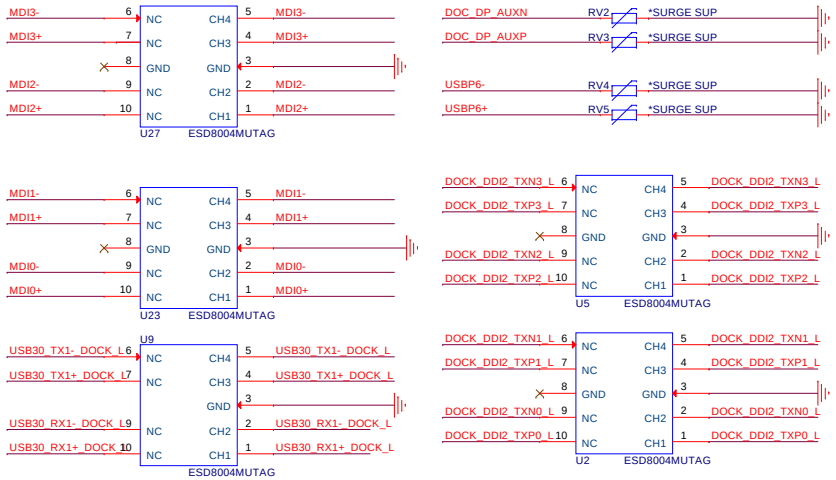
13,19,22,25,29,32,37,41,42,53 +3VPCU
20,22,30,31,49 +5V
4,19,26,27,28,32,37,42,43,46,47,48,49,50,52 +5VS5
53 DOCK-PWR20-IN

33



DP HPD SENSE



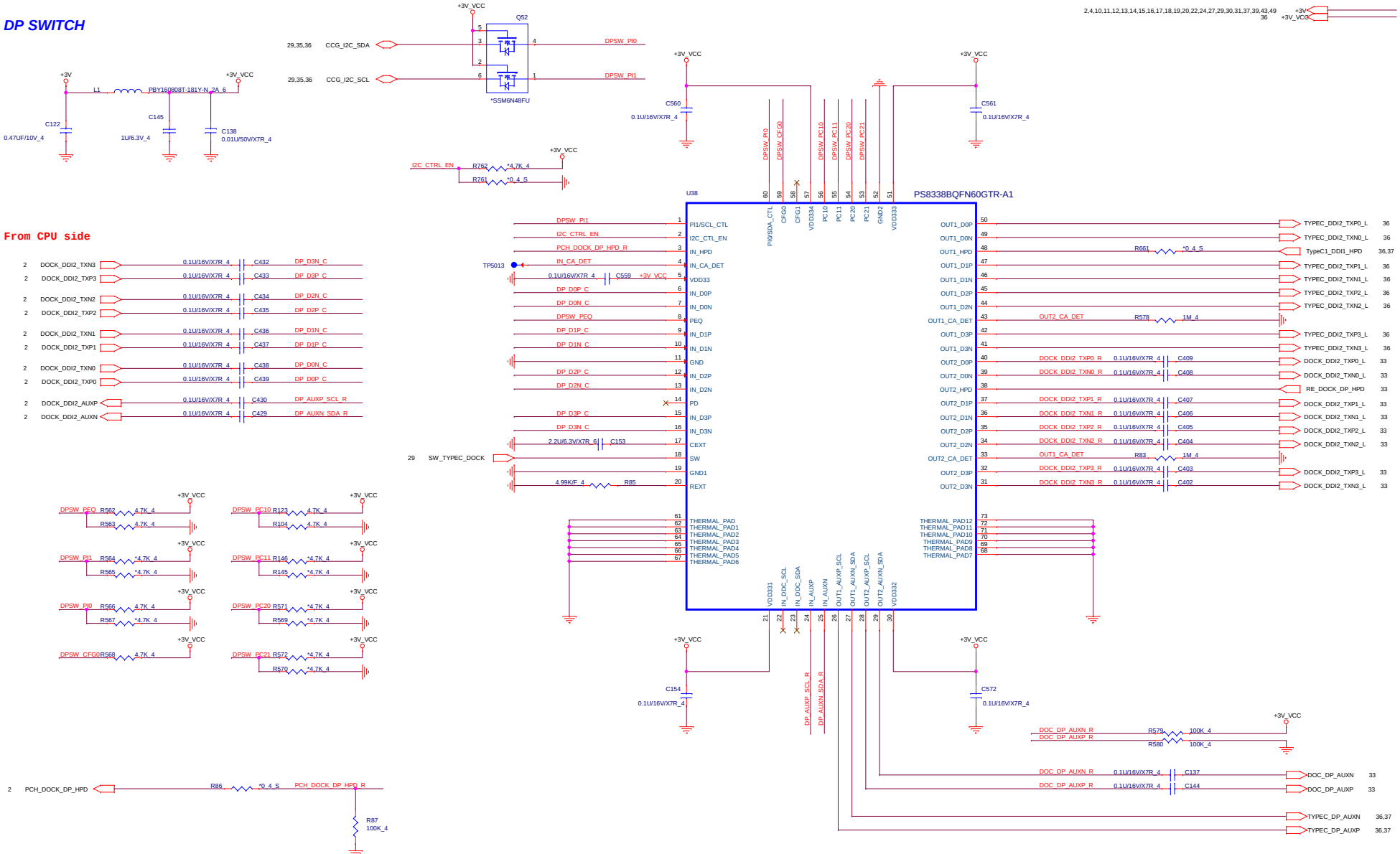


Quanta Computer Inc.

PROJECT: PS9

Size	Document Number	Rev
Custom	PROLINK	1A
Date: Wednesday, July 27, 2016	Sheet 33 of 55	

DP SWITCH



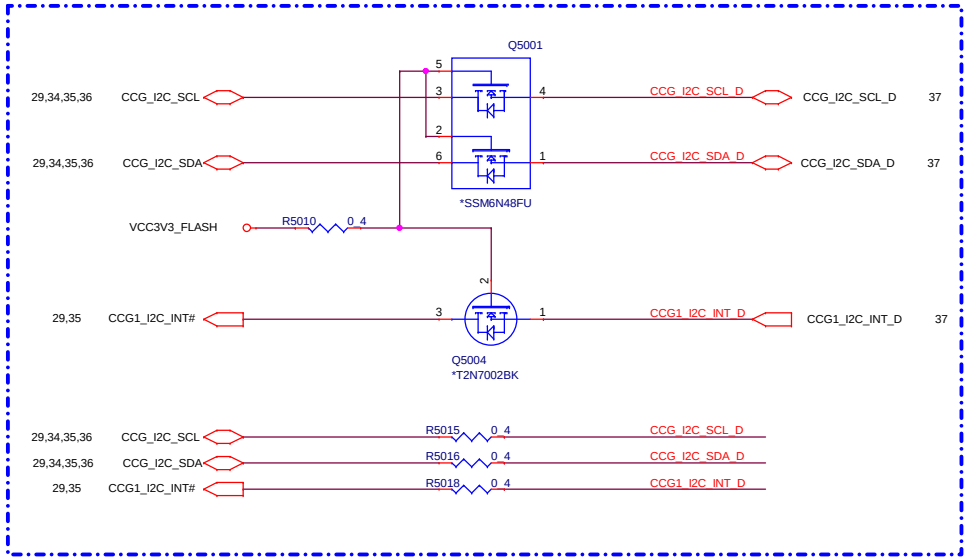
SW_TYPEC_DOCK	Display Priority
Low	USB Type-C
High	Docking Station

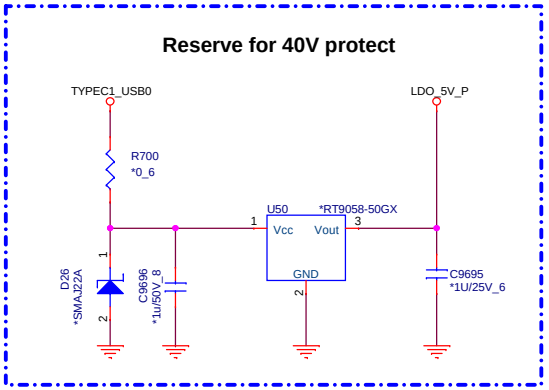
Quanta Computer Inc.
PROJECT: PS9

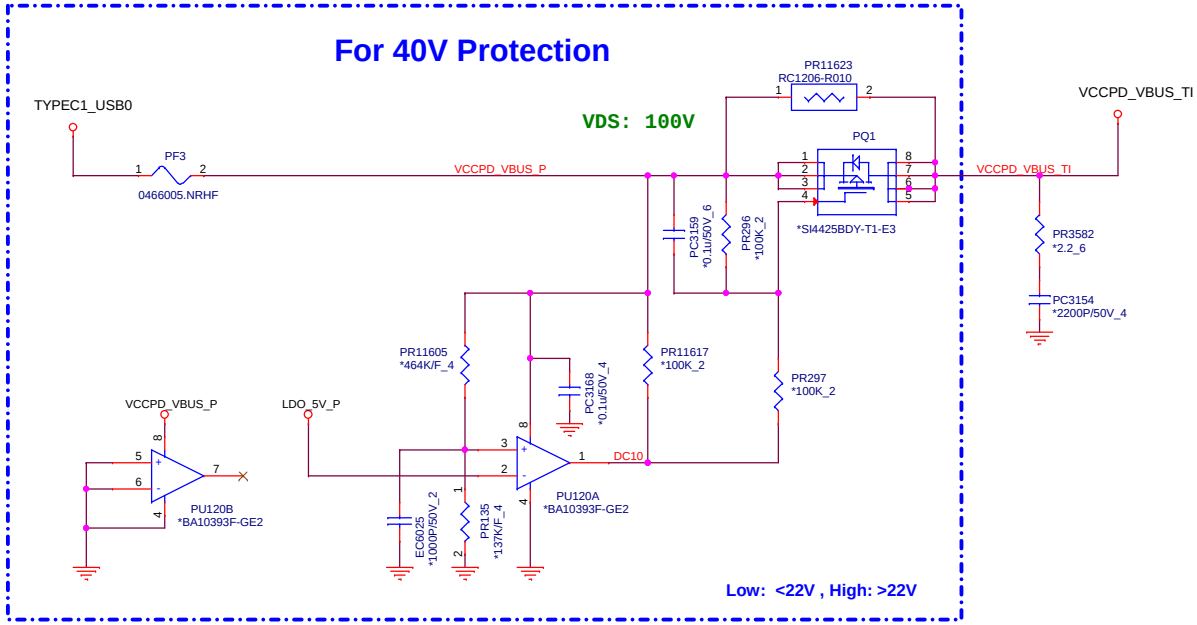
Size	Document Number	Rev
Custom		1A

Date: Wednesday, July 27, 2016 Sheet 34 of 55

38 TYPEC1_USB0
37,53 VCCPD_VBUS_TI
37,38 VCC3V3_FLASH







Quanta Computer Inc.
PROJECT: PS9

Size	Document Number	Rev
Custom	VBUS 40V PROTECT	1A

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PS8743B PIN Control Mode

PS8743 Mode Selection			
CE_DP	CE_USB	FLIP	
L	L	L	Chip Power Down
L	L	H	Chip Power Down
L	H	L	USB only on SS1 channels
L	H	H	USB only on SS2 channels
H	L	L	DP only; ML0 on SSRX2
H	L	H	DP only; ML0 on SSRX1
H	H	L	USB+2lanes DP;DP ML0 on SSRX2
H	H	H	USB+2lanes DP;DP ML0 on SSRX1

DisplayPort Source

USB3.0 HOST

DisplayPort Source

TUSB546-DCI : AL000546009

PS8743BQFN40GTR-B0

C9718: POP for TI

R5119: POP for TI

R5117: POP for TI

3 PAD DESIGN(R5096/R5012 & R5093/R5017)

R5118: RESERVE for TI

R5039: RESERVE for TI

R632: TBD for TI

3 PAD DESIGN

	PS8743B	TUSB546
PIN29	4.7K	4.7K
PIN2	4.99K	DEPOP
PIN23	R5091:POP	R5091:POP
PIN35	R5092:POP	R5106:POP
PIN38	R5093:POP	R5107:POP
PIN21	R5098:POP	R5100:POP
PIN22	R5099:POP	R5101:POP
R5119	Depop	POP
R5116	POP	Depop
C9791	POP	Depop
R5117	Depop	POP
R5060	POP	Depop

USB HOST facing TX channel De-emphasis setting. Internally pull down at 150kΩ. Tolerant to VDD_DCI only.
SSDE =
L: -3.5dB Output De-emphasis(default)
H: -6dB Output De-emphasis

USB Type-C connector facing TX channel De-emphasis setting. Internally pull down at 150kΩ. Tolerant to VDD_DCI only.
CDE =
L: -3.5dB Output De-emphasis(default)
H: -6dB Output De-emphasis

DCI mode configuration pin; Internally tied to VDD33/2, 3.3V I/O.
DCICFG =
L: DCI mode disabled
H: DCI mode enabled
M: Automatic DCI mode entering enabled (

USB Type-C connector facing RX channel receiver equalization setting; Internally tied to VDD33/2, 3.3V I/O.
CEQ =
L: Compensation for channel loss up to 7dB
H: Compensation for channel loss up to 18.5dB
M: Compensation for channel loss up to 11.5dB(default)

DP Receiver equalization setting; Internal tied to VDD33/2, 3.3V I/O.
DPEQ =
L: Compensation for channel loss up to 7dB
H: Compensation for channel loss up to 14.5dB
M: Compensation for channel loss up to 10.5dB(default)

*SSM6N48FU

Quanta Computer Inc.
PROJECT: PS9

Size	Document Number	Rev
Custom	PS8743B PIN CONTROL	1A
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TPS65982(D)

PP_HV-->Tie to GND if unused

45W ADAPTER ONLY

W = 120 mils

W = 120 mils

W = 200 mils

I2C_ADDR
'0' - Sets ACE as Primary
ADDR:0X00

EC-FVT-09

Primary

Config:7 (0.7~1)

I2C_2 To EC

RESERVE CONNECT TO EC

Tie RPD_Gn to C_CCn pins to support no-power or dead-battery modes

USB2.0 ESD

8Mbit Flash (Mutual for AR and ACE)

Vender	Size	P/N
EON	1MB	AKE3GZN0Q03 (EN25Q80B-104GIP)
Winbond	1MB	AKE3GGN0N02 (W25Q80DVSNIG)
MXIC	1MB	AKE3GFP0Z01 (MX25L8006EM1I-12G)

Quanta Computer Inc.
PROJECT: PS9
Size | Document Number | Rev 1A
Date: Wednesday, July 27, 2016 Sheet 37 of 55

Type C1_HSIO_ ESD

35,37 VCC3V3_FLASH
35 TYPEC1_USB0

36 TYPEC1_TX1P_C
36 TYPEC1_TX1N_C
TYPEC1_TX1P_C — R640 0_4 — TYPEC1_TX1P_R
TYPEC1_TX1N_C — R641 0_4 — TYPEC1_TX1N_R

36 TYPEC1_RX2N
36 TYPEC1_RX2P
TYPEC1_RX2N — R644 0_4 — TYPEC1_RX2N_R
TYPEC1_RX2P — R645 0_4 — TYPEC1_RX2P_R

36 TYPEC1_TX2P_C
36 TYPEC1_TX2N_C
TYPEC1_TX2P_C — R646 0_4 — TYPEC1_TX2P_R
TYPEC1_TX2N_C — R648 0_4 — TYPEC1_TX2N_R

36 TYPEC1_RX1N
36 TYPEC1_RX1P
TYPEC1_RX1N — R651 0_4 — TYPEC1_RX1N_R
TYPEC1_RX1P — R652 0_4 — TYPEC1_RX1P_R

TYPEC1_USB0 — C612 0.1U/25V_4 — C613 0.1U/25V_4

CN21
TYPEC1_USB0 — A4 A9 VBUS VBUS1 — VBUS2 VBUS3 B4 B9 — TYPEC1_USB0
TYPEC1_TX1P_R — A2 TX1P — RX1P B11 — TYPEC1_RX1P_R
TYPEC1_TX1N_R — A3 TX1N — RX1N B10 — TYPEC1_RX1N_R
37 TYPEC_USB1D+ — TYPEC_USB1D+ A6 DP1 — DN2 B7 TYPEC_USB2D- — TYPEC_USB2D- 37
37 TYPEC_USB1D- — TYPEC_USB1D- A7 DN1 — DP2 B6 TYPEC_USB2D+ — TYPEC_USB2D+ 37
TYPEC1_RX2N_R — A10 RX2N — TX2N B3 — TYPEC1_TX2N_R
TYPEC1_RX2P_R — A11 RX2P — TX2P B2 — TYPEC1_TX2P_R
TYPEC1_SBU1 — A8 RFU1 — RFU2 B8 — TYPEC1_SBU2
TypeC1_CCG1_CC1 — A5 CC1 — CC2 B5 — TypeC1_CCG1_CC2
GND4 13, GND5 14, GND6 15, GND7 16, GND8 17, GND9 18, GND10 19, GND11 20, GND12 21, GND13 22, GND14 23, GND15 24
A1 GND, A12 GND1, B1 GND2, B12 GND3
TYPE_C_CONN

TYPEC1_SBU2 — R643 2M_2
TYPEC1_SBU1 — R642 2M_2

Close to connector CN21
TYPEC1_USB0 — C1019 1000P/50V/X7R_4

TYPEC1_USB0 — EC6028 AZ4520-01F

U53
TYPEC1_RX1N_R — 9 LINE-2 — LINE-1 1 — TYPEC1_RX1P_R
TYPEC1_TX1N_R — 8 LINE-4 — LINE-3 2 — TYPEC1_TX1P_R
GND 3
TYPEC1_TX2N_R — 7 LINE-5 — LINE-6 4 — TYPEC1_TX2P_R
TYPEC1_RX2N_R — 6 LINE-7 — LINE-8 5 — TYPEC1_RX2P_R
AZ1043-08F

U54
TYPEC_USB2D+ — 9 LINE-2 — LINE-1 1 — TYPEC_USB2D-
8 LINE-4 — LINE-3 2
GND 3
TYPEC_USB1D+ — 7 LINE-5 — LINE-6 4 — TYPEC_USB1D-
TYPEC1_SBU2 — 6 LINE-7 — LINE-8 5 — TYPEC1_SBU1
AZ1045-08F

EC-SIT-05
EC-FVT-01

TypeC1_CCG1_CC1
TypeC1_CCG1_CC2
EC6030 AZ4520-01F
EC6029 AZ4520-01F
EC-SIT-05

U5002
TYPEC_USB1D+ — 20 D4
TYPEC_USB1D- — 19 D3
18 GND2
TYPEC_USB2D- — 17 D2
TYPEC_USB2D+ — 16 D1
PD_TYPEC1_SBU1 — 1 SBU1 — C_SBU1 15 — TYPEC1_SBU1
PD_TYPEC1_SBU2 — 2 SBU2 — C_SBU2 14 — TYPEC1_SBU2
3 GND — VBIAS 13 — C9789 *1U/6.3V_2
PD_TYPEC1_CCG1_CC1 — 4 CC1 — C_CC1 12 — TypeC1_CCG1_CC1
PD_TYPEC1_CCG1_CC2 — 5 CC2 — C_CC2 11 — TypeC1_CCG1_CC2
VPWR 6, FLT 7, GND1 8, RPD_G1 9, RPD_G2 10, EGND 21
*TPD8S300RUKR
VCC3V3_FLASH — R5057 *0_2
C9790 *1U/6.3V_2
R5058 *100K_4
TypeC1_CCG1_CC1, TypeC1_CCG1_CC2
VCC3V3_FLASH
EC-SIT-04

EC-FVT-01 EC-SIT-04
36,37 PD_TYPEC1_SBU1 — PD_TYPEC1_SBU1 — R5053 0_2 — TYPEC1_SBU1
36,37 PD_TYPEC1_SBU2 — PD_TYPEC1_SBU2 — R5054 0_2 — TYPEC1_SBU2
37 PD_TYPEC1_CCG1_CC1 — PD_TYPEC1_CCG1_CC1 — R5055 0_2 — TypeC1_CCG1_CC1
37 PD_TYPEC1_CCG1_CC2 — PD_TYPEC1_CCG1_CC2 — R5056 0_2 — TypeC1_CCG1_CC2

Quanta Computer Inc.
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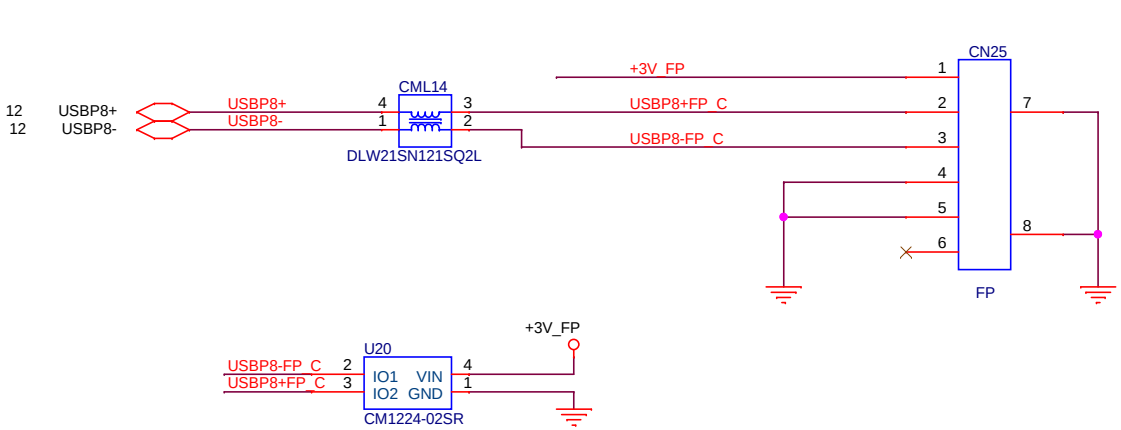
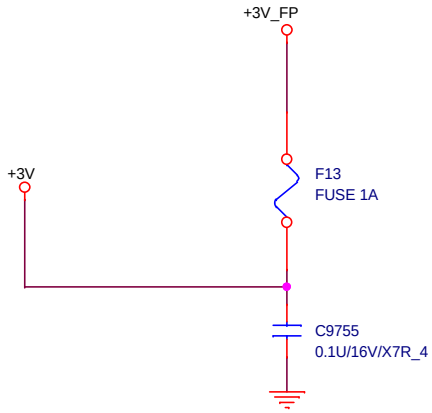
Date: Wednesday, July 27, 2016 | Sheet 38 of 55

USB INTERFACE

2,4,10,11,12,13,14,15,16,17,18,19,20,22,24,27,29,30,31,34,37,43,49 +3V





Quanta Computer Inc.		
PROJECT: PS9		
Size	Document Number: FINGER PRINT	Rev: 1A
Date: Wednesday, July 27, 2016	Sheet 39 of 55	

H7
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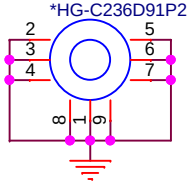

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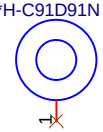

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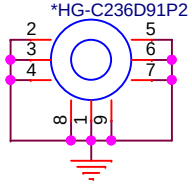

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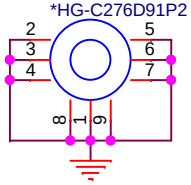

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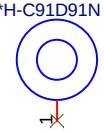

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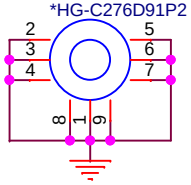

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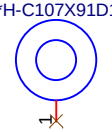

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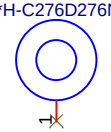

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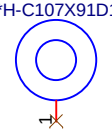

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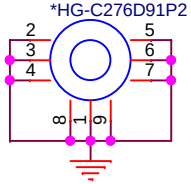

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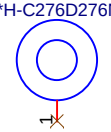

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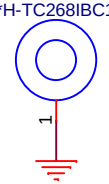

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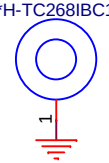

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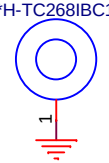

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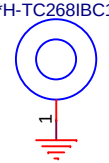

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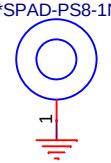

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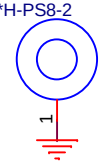
*H-PS8-2



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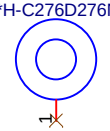

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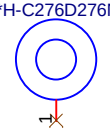

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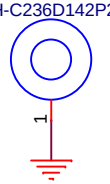

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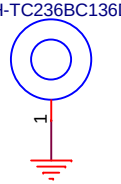

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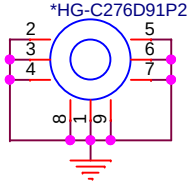

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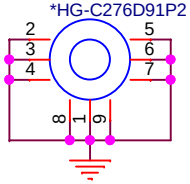

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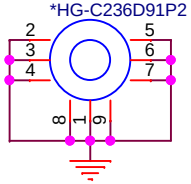

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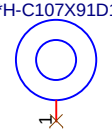

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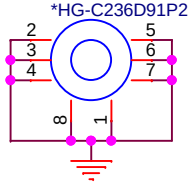

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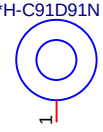

Quanta Computer Inc.

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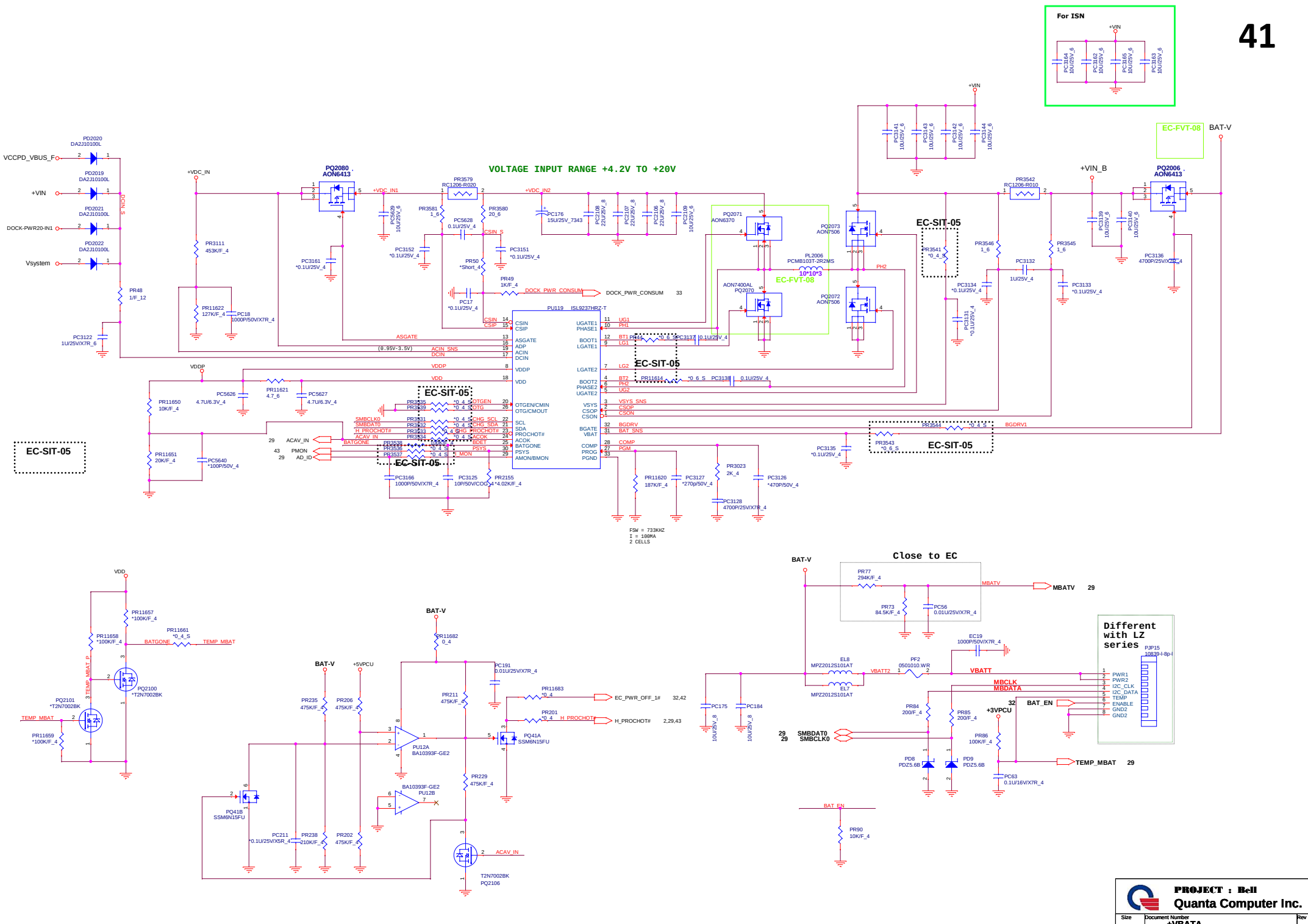
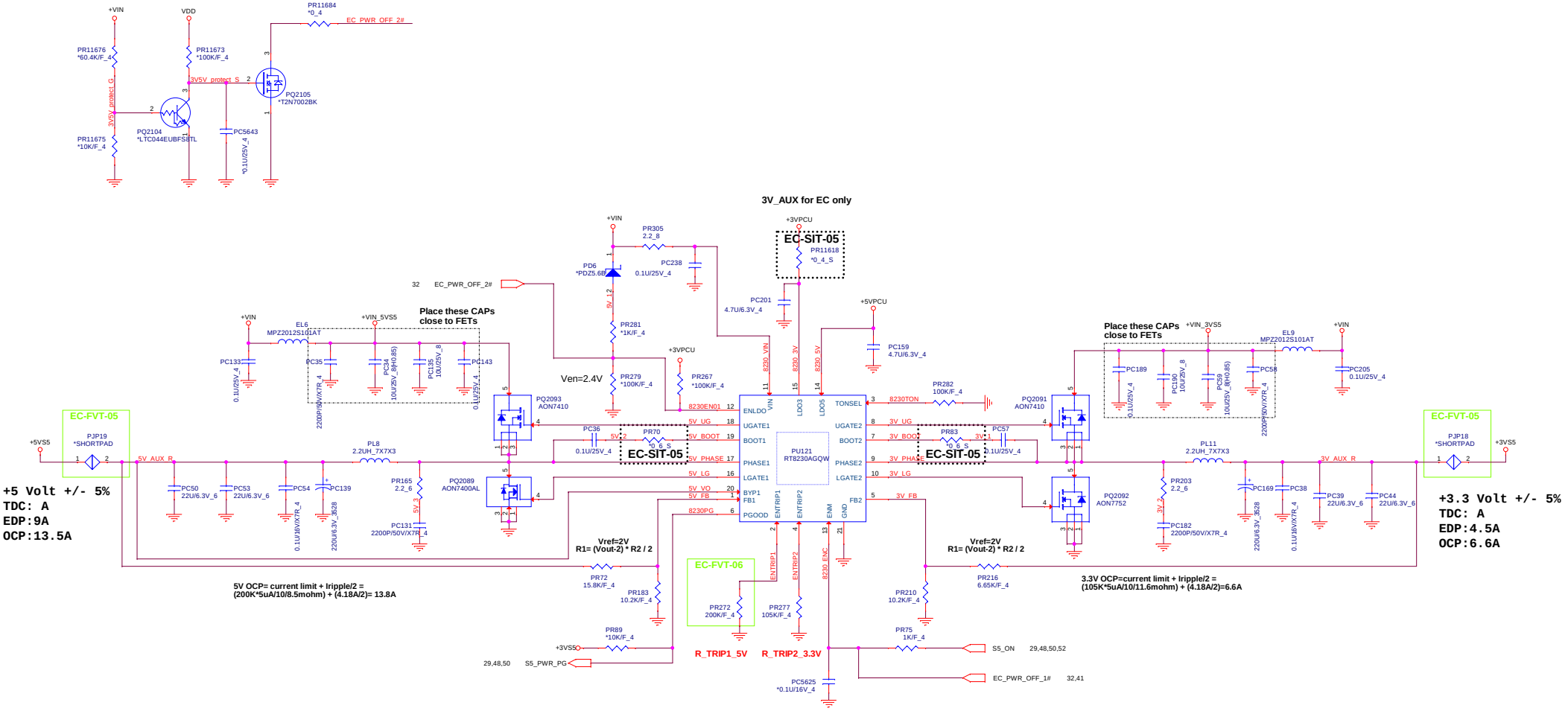

For ISN
+VIN
PC3164 10U/25V_6
PC3162 10U/25V_6
PC3165 10U/25V_6
PC3163 10U/25V_6
VOLTAGE INPUT RANGE +4.2V TO +20V
EC-SIT-05
EC-FVT-08
BAT-V
+VIN_B
+VDC_IN
VCCPD_VBUS_F
DOCK-PWR20-IN1
Vsystem
PQ2080 AON6413
PQ2006 AON6413
PQ2071 AON6370
PQ2073 AON7506
PQ2072 AON7506
AON7400AL PQ2070
PL2006 PCMB103T-2R2MS
PU119 ISL9237HRZ-T
PR3579 RC1206-R020
PR3542 RC1206-R010
PR3581 1_6
PR3580 20_6
PC5628 0.1U/25V_4
PR50 *Short_4
PR49 1K/F_4
PC17 *0.1U/25V_4
PR3111 453K/F_4
PR11622 127K/F_4
PC18 1000P/50V/X7R_4
PR48 1/F_12
PC3122 1U/25V/X7R_6
PC3161 *0.1U/25V_4
PC3152 *0.1U/25V_4
PC3151 *0.1U/25V_4
PC176 15U/25V_7343
PC3132 1U/25V_4
PC3134 *0.1U/25V_4
PC3133 *0.1U/25V_4
PC3136 4700P/25V/X7R_4
PC3121 *0.1U/25V_4
PR3541 *0_4_S
PR3546 1_6
PR3545 1_6
PC3139 10U/25V_6
PC3140 10U/25V_6
PR11650 10K/F_4
PR11651 20K/F_4
PC5626 4.7U/6.3V_4
PR11621 4.7_6
PC5627 4.7U/6.3V_4
PC5640 *100P/50V_4
PR3535 *0_4_S OTGEN
PR3539 *0_4_S OTG
PR3531 *0_4_S CHG_SCL
PR3532 *0_4_S CHG_SDA
PR3533 *0_4_S CHGROCHOT#
PR3534 *0_4_S ACOK
PR3538 *0_4_S BDET
PR3536 *0_4_S PSYS
PR3537 *0_4_S I_MON
PC3166 1000P/50V/X7R_4
PC3125 10P/50V/COG_4
PR2155 *4.02K/F_4
PR11620 187K/F_4
PC3127 *270P/50V_4
PR3023 2K_4
PC3126 *470P/50V_4
PC3128 4700P/25V/X7R_4
PC3135 *0.1U/25V_4
PR3544 *0_4_S
PR3543 *0_6_S
BGDRV1
PR11614 *0_6_S
PC3137 0.1U/25V_4
PC3141 10U/25V_6
PC3143 10U/25V_6
PC3142 10U/25V_6
PC3144 10U/25V_6
PC3129 10U/25V_6
PC3108 22U/25V_8
PC3107 22U/25V_8
PC3106 22U/25V_8
PC3105 10U/25V_6
PD2020 DA2J10100L
PD2019 DA2J10100L
PD2021 DA2J10100L
PD2022 DA2J10100L
DCIN_S
ASGATE
ACIN_SNS
DCIN
VDDP
VDD
SMBCLK0
SMBDAT0
H_PROCHOT#
ACAV_IN
BATGONE
PMON
AD_ID
DOCK_PWR_CONSUM
PH2
BT1
LG1
BT2
PH2
LG2
UG2
VSYS_SNS
CSOP
CSON
BGDRV
BAT_SNS
COMP
PGM
FSW = 733KHZ
I = 100MA
2 CELLS
Close to EC
PR77 294K/F_4
PR73 84.5K/F_4
PC56 0.01U/25V/X7R_4
MBATV
EC19 1000P/50V/X7R_4
EL8 MPZ2012S101AT
EL7 MPZ2012S101AT
PF2 0501010.WR
VBATT
VBATT2
MBCLK
MBDATA
BAT_EN
+3VPCU
PR84 200/F_4
PR85 200/F_4
PR86 100K/F_4
PD8 PDZ5.6B
PD9 PDZ5.6B
PC63 0.1U/16V/X7R_4
TEMP_MBAT
PR90 10K/F_4
PC175
PC184
SMBDAT0
SMBCLK0
Different with LZ series
PJP15 10039-i-8p
PWR1
PWR2
I2C_CLK
I2C_DATA
TEMP
ENABLE
GND2
GND2
PR11657 *100K/F_4
PR11658 *100K/F_4
PR11661 *0_4_S
PQ2100 *T2N7002BK
PQ2101 *T2N7002BK
PR11659 *100K/F_4
PR11682 0_4
PC191 0.01U/25V/X7R_4
PR11683 *0_4
EC_PWR_OFF_1#
PR201 *0_4
PQ41A SSM6N15FU
PU12A BA10393F-GE2
PU12B
PR235 475K/F_4
PR206 475K/F_4
PR211 475K/F_4
PR229 475K/F_4
PR202 475K/F_4
PC211 *0.1U/25V/X5R_4
PR238 210K/F_4
PQ41B SSM6N15FU
T2N7002BK PQ2106

19,41,43,44,45,46,47,48,51,52 +VIN
13,19,22,25,29,32,33,37,41,53 +3VPCU
4,10,12,15,16,19,21,23,25,27,28,31,32,36,37,48,49,50,52 +3VS5
4,19,26,27,28,32,33,37,43,46,47,48,49,50,52 +5VS5



Power On sequencing

ENLD0	ENM	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 1V	LOW	ON	ON	ON	OFF	OFF
> 1V	> 2.3V	ON	ON	ON	ON	ON

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Quanta Computer Inc.

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	V5A_V3P3A	1A
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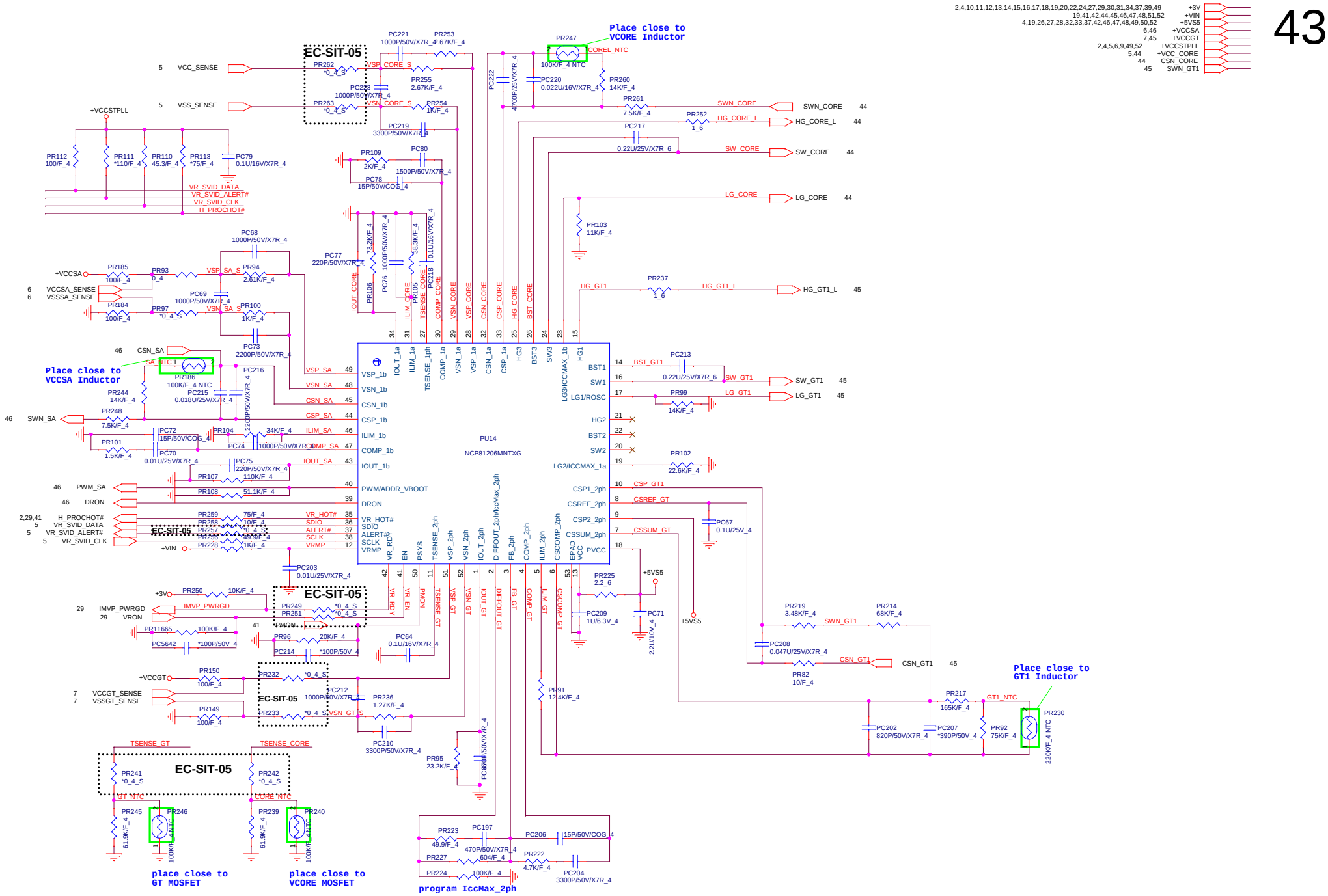

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Quanta Computer Inc.	
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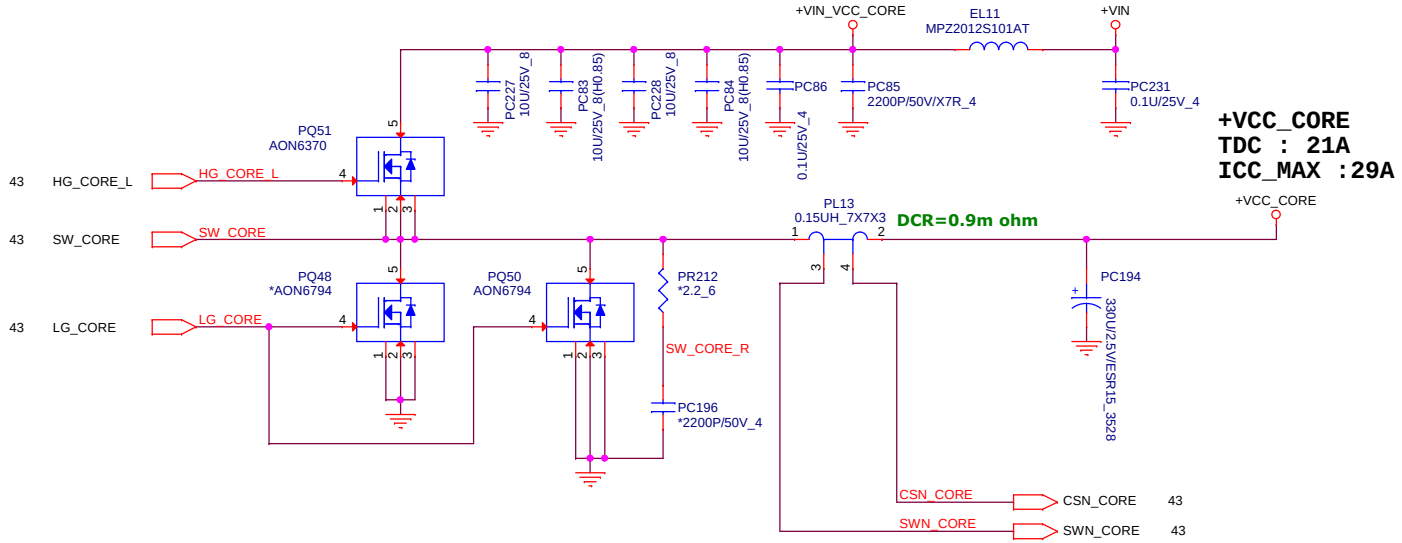
19,41,42,43,45,46,47,48,51,52 +VIN
5 +VCC_CORE

44



+VCC_CORE
TDC : 21A
ICC_MAX :29A

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Quanta Computer Inc.			
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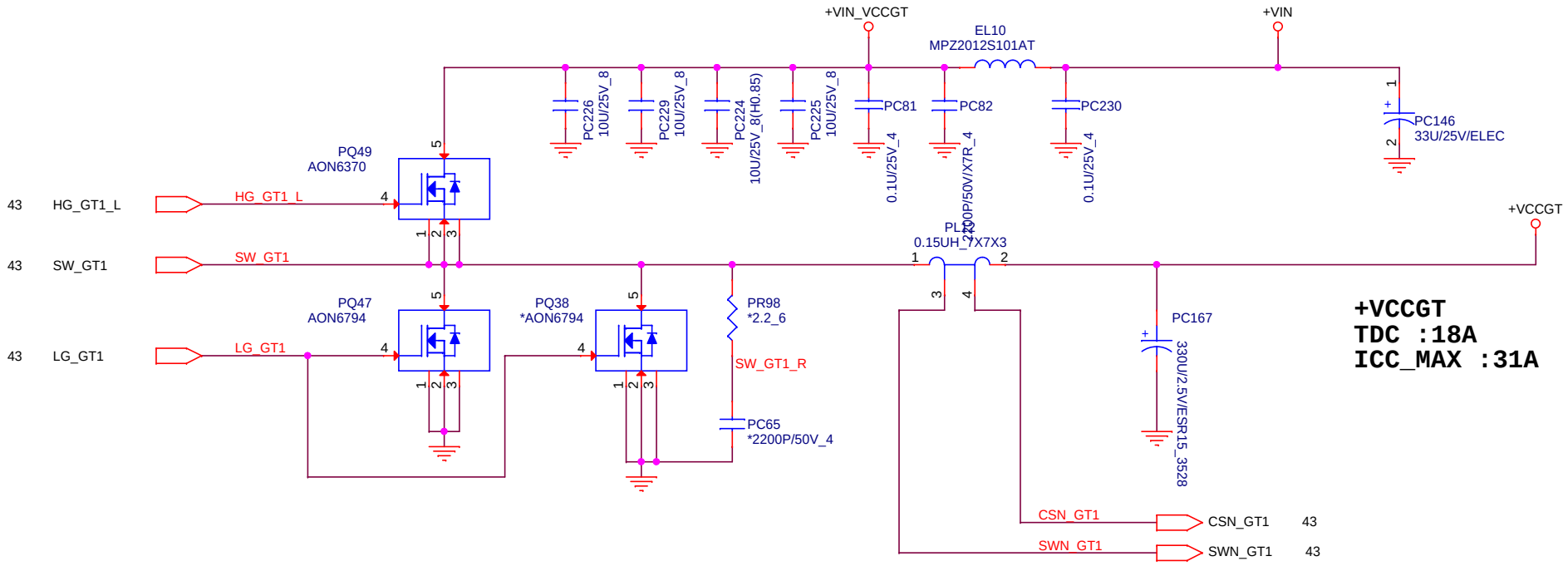
19,41,42,43,44,46,47,48,51,52 +VIN
7,43 +VCCGT



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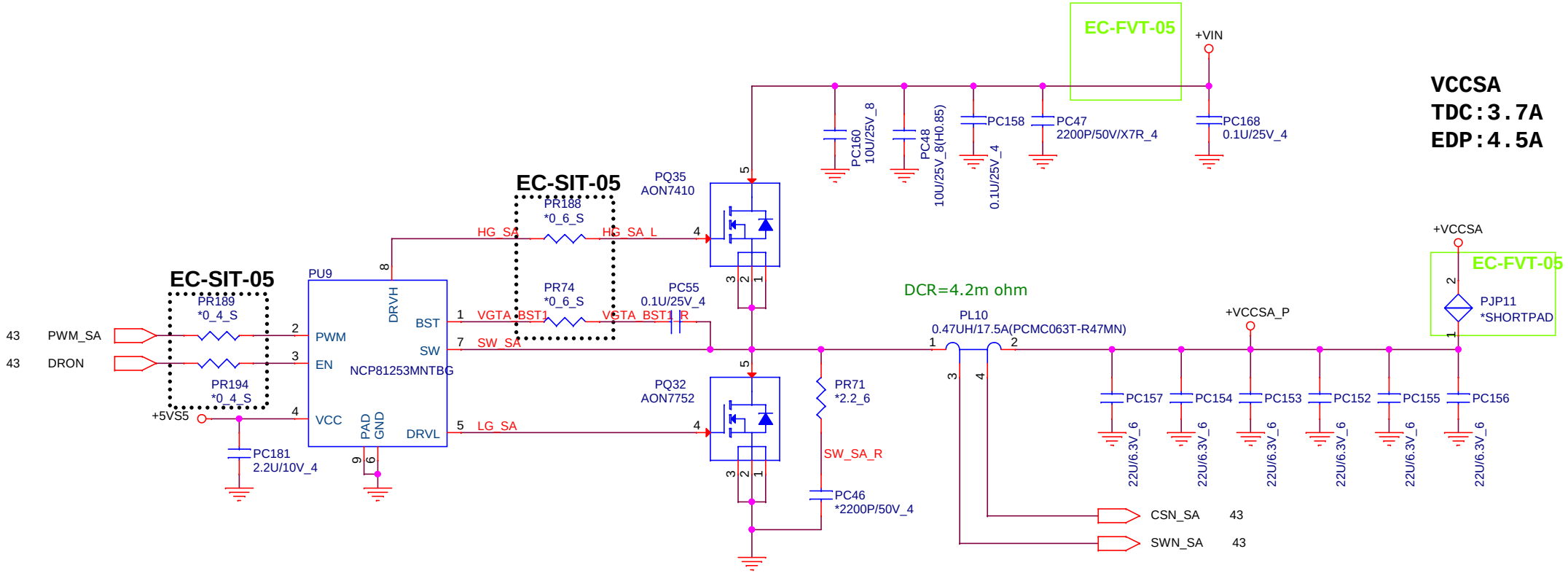
VCCSA

19,41,42,43,44,45,47,48,51,52 +VIN
6,43 +VCCSA
4,19,26,27,28,32,33,37,42,43,47,48,49,50,52 +5VS5



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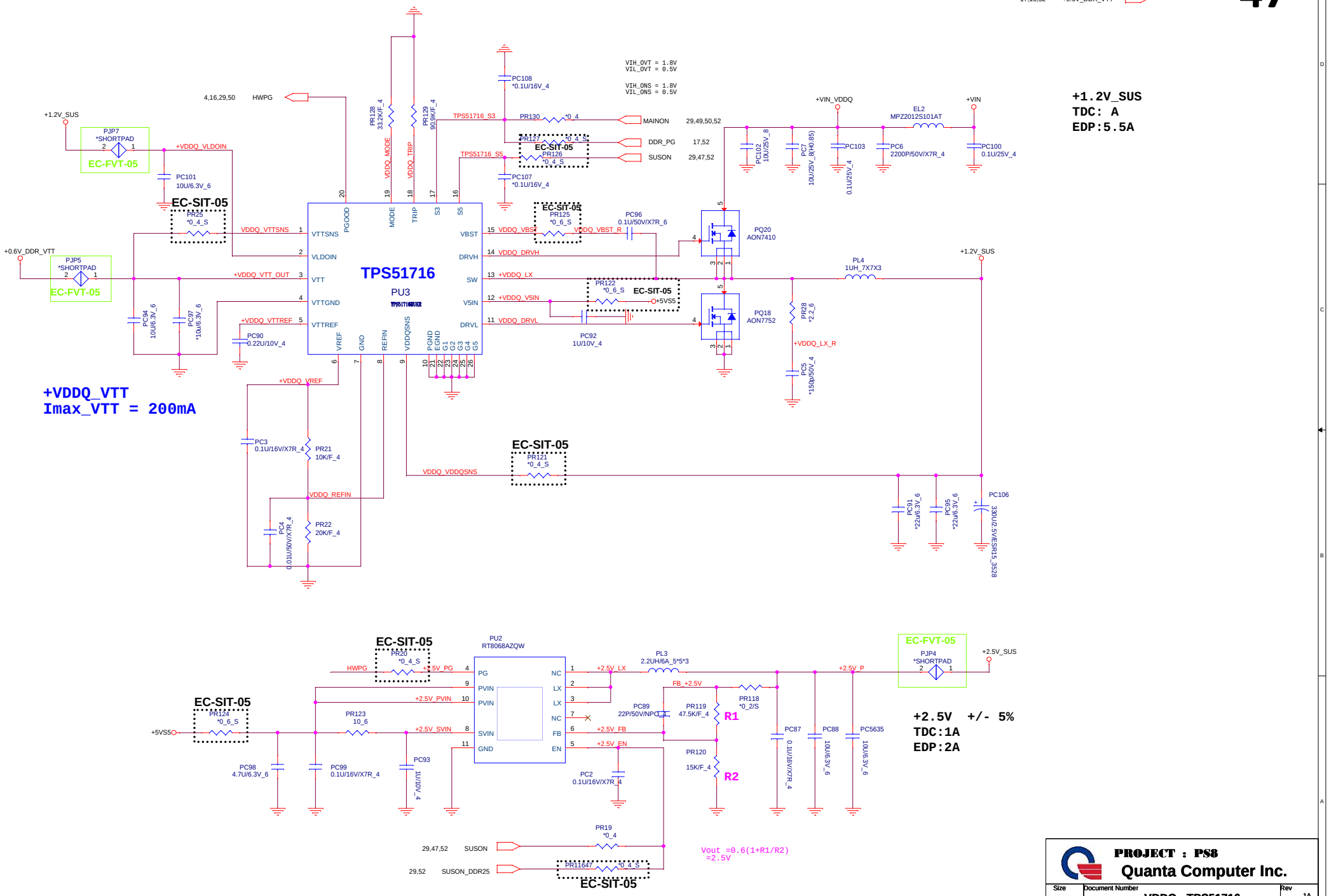
Fsw=500kHz

VR PAGE: +VDDQ

19,41,42,43,44,45,46,48,51,52 +VIN
4,19,26,27,28,32,33,37,42,43,46,48,49,50,52 +5VS5
2,4,10,11,12,13,14,15,16,17,18,19,20,22,24,27,29,30,31,34,37,39,43,49 +3V
3,6,17,18,52 +1.2V_SUS
17,18,52 +0.6V_DDR_VTT



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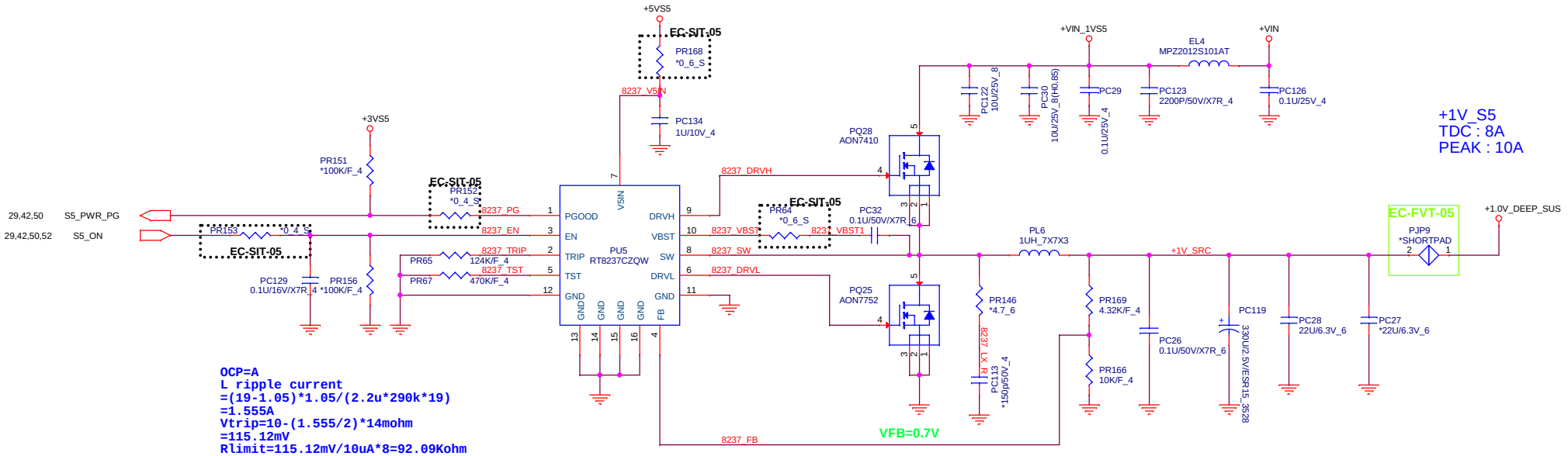
V1P0A (RT8237CZQW)

9,13,15,16,49,52 +1.0V_DEEP_SUS
19,41,42,43,44,45,46,47,51,52 +VIN
4,19,26,27,28,32,33,37,42,43,46,47,49,50,52 +5VS5
4,10,12,15,16,19,21,23,25,27,28,31,32,36,37,42,49,50,52 +3VS5



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	+1.0V_DEEP_SUS		1A
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2,4,10,11,12,13,14,15,16,17,18,19,20,22,24,27,29,30,31,34,37,39,43 +3V
20,22,30,31,33 +5V
4,19,26,27,28,32,33,37,42,43,46,47,48,50,52 +5VS5
4,10,12,15,16,19,21,23,25,27,28,31,32,36,37,42,48,50,52 +3VS5
9,13,15,16,48,52 +1.0V_DEEP_SUS
2,4,5,6,9,43,52 +VCCSTPLL
2,4,6,16,52 +VCCIO

Imax=5.26A
Pd: ?W

+3VS5 PC174 0.1U/16V/X7R_4
+5VS5 PC128 0.1U/16V/X7R_4
+3V PR221 *0_8_S EC-SIT-05 +3V_S2
PC195 *10U/6.3V_6
PC188 0.1U/16V/X7R_4
PU11 RT9740AGQW
VIN1 VIN1 VIN2 VIN2
VOUT1 VOUT1 OUT2 OUT2
GND GND
VBIAS
ON1 ON2 CT1 CT2
+5VS5 PC179 0.1U/16V/X7R_4
29,47,50,52 MAINON PR198 *0_4_S EC-SIT-05
PC178 *0.1U/16V_4
PC198 1000P/50V/X7R_4
PC199 1000P/50V/X7R_4
PC180 *0.1U/16V_4
EC-SIT-05 PR190 *0_4_S MAINON
+5V_S2 EC-SIT-05 PR218 *0_6_S +5V
PC192 0.1U/16V/X7R_4
PC200 *10U/6.3V_6

Imax=1.58A
Pd: ?W

+1.0V_DEEP_SUS
PC171 1U/6.3V_4
PQ42 AON7410
+VCCIO_P
EC-FVT-05 PJP14 *SHORTPAD +VCCIO
PC185 0.1U/16V/X7R_4
PC186 *10U/6.3V_6
PR78 *0_4_S EC-SIT-05
52 MAINON_G PR88 *0_4_S
PC62 *0.1U/16V_4
PU10 *AOZ1335DI
VIN VIN VIN VOUT
+3VS5 VBIAS
PC172 *0.1U/16V_4
MAINON EC-SIT-05 PR196 *0_4 MAINON_VCCIO
ON GND
PC173 *0.1U/16V_4

+VCCIO
TDC : ?A
PEAK : 3.8A

<= 65usec full load ready

+1.0V_DEEP_SUS
PC132 0.1U/16V/X7R_4
PQ30 AON7410
52 SUSON_G1 PR177 *0_4_S EC-SIT-05 +VCCSTG_ON PR167 *0_4_S EC-SIT-05 +VCCSTG_ON_G
PC151 *1000P/50V_4
+VCCSTPLL_P PR170 *0_6_S EC-SIT-05 +VCCSTPLL
PC149 0.1U/16V/X7R_4
PC150 *10U/6.3V_6

<= 65usec full load ready

TDC : 0.16A

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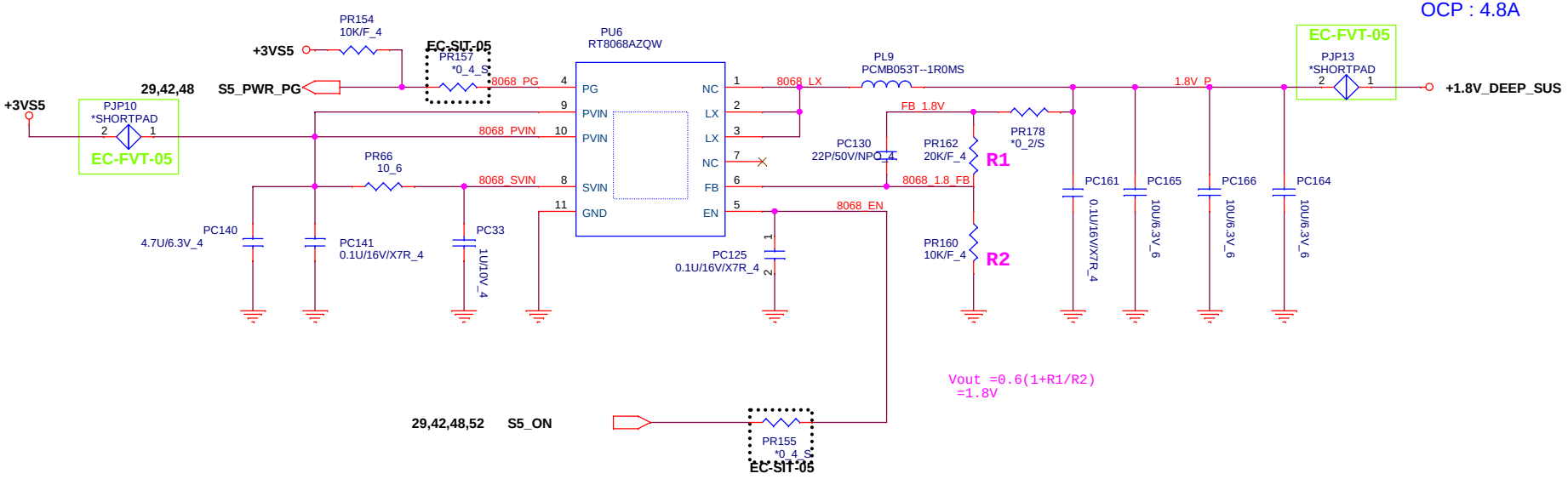
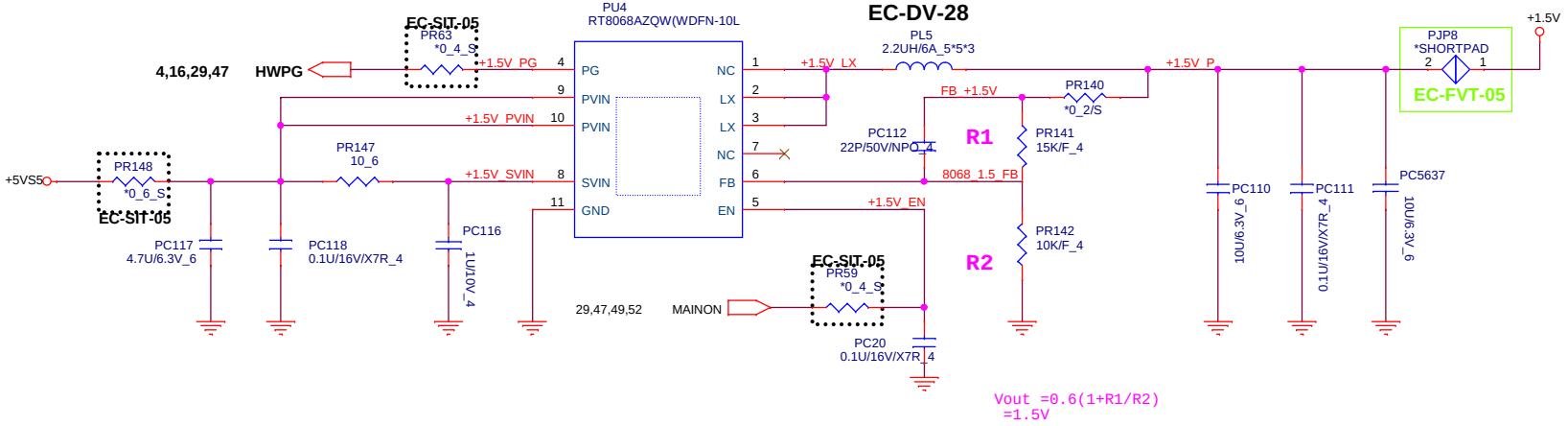
V1P8A (RT8068A)

1.8V_S5
Fsw : 900KHz
PEAK : 0.27A
OCP : 4.8A



+1.5V +/- 5%
TDC:1A
EDP:2A



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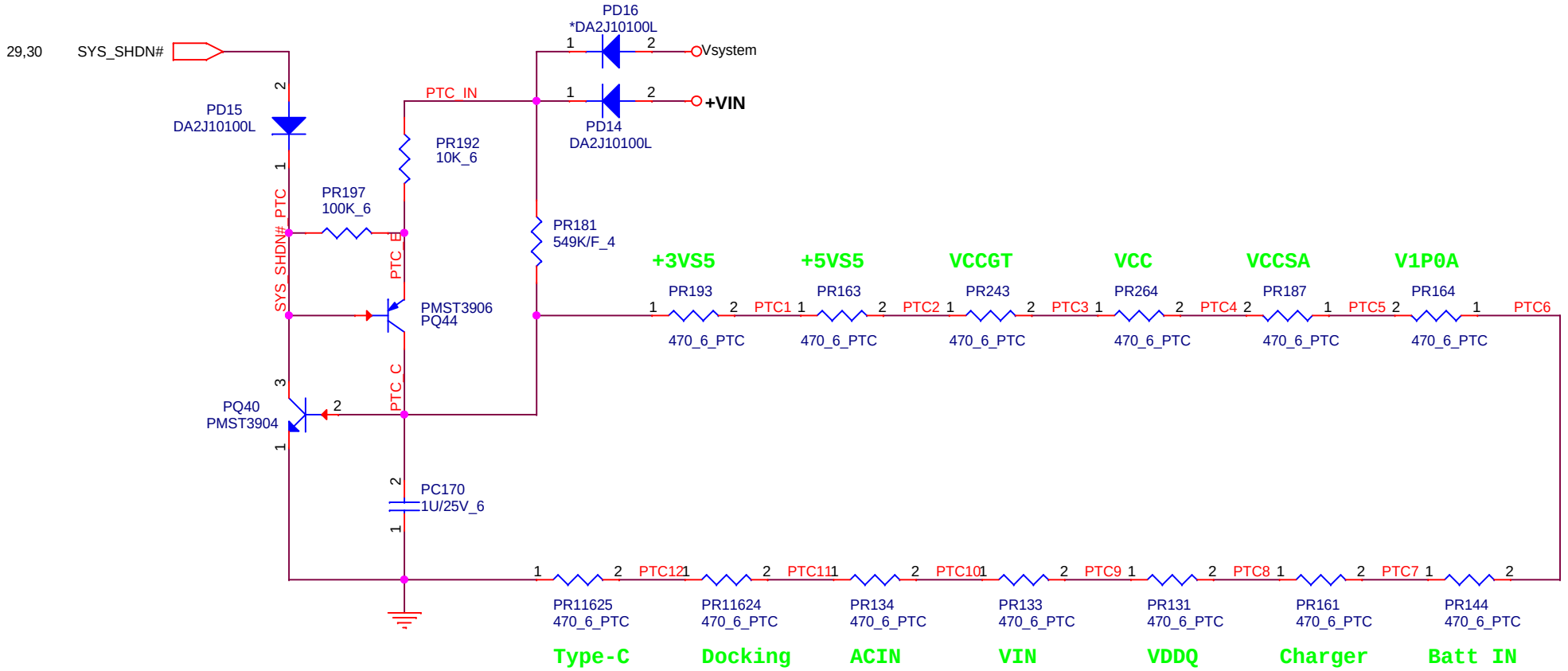

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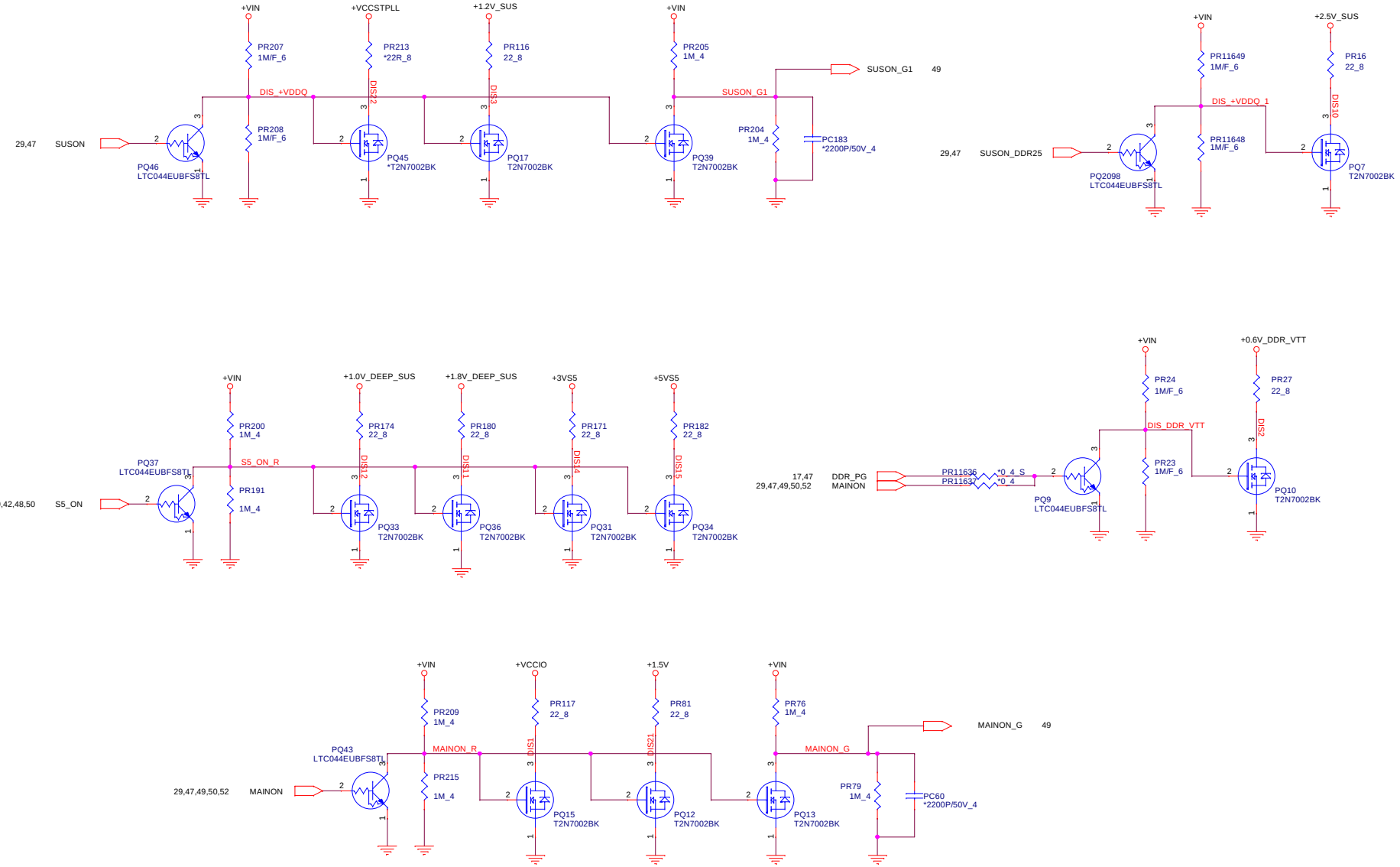
DISCHARGE



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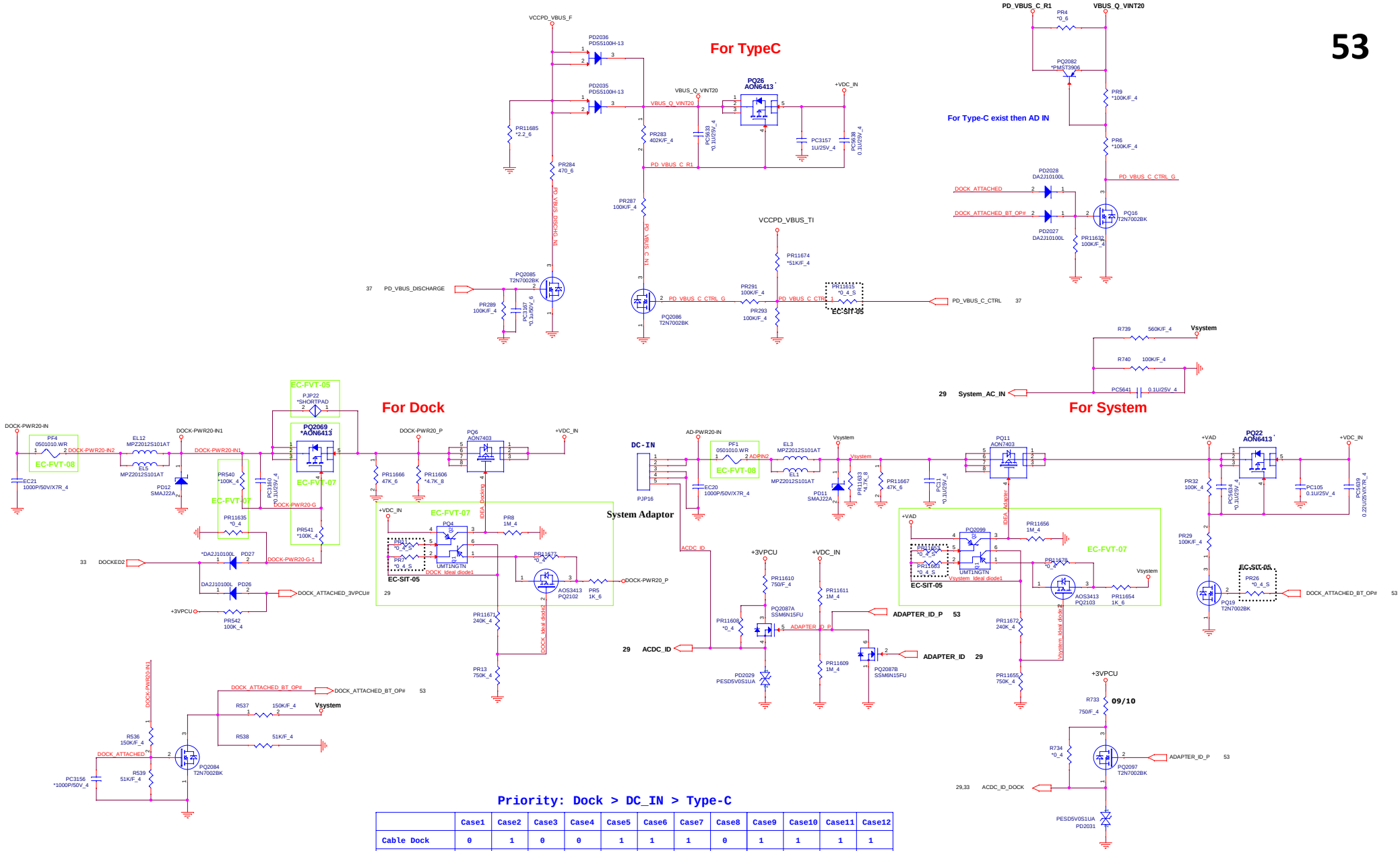

Priority: Dock > DC_IN > Type-C

	Case1	Case2	Case3	Case4	Case5	Case6	Case7	Case8	Case9	Case10	Case11	Case12
Cable Dock	0	1	0	0	1	1	1	0	1	1	1	1
AD on Dock	0	0	0	0	1	0	0	0	1	1	0	1
AD on Sys	0	0	1	0	0	1	0	1	1	0	1	1
AD on Type-C	0	0	0	1	0	0	1	1	0	1	1	1
Power Source	Batt	Batt	AD on Sys	AD on Type-C	AD on Dock	AD on Sys	AD on Type-C	AD on Sys	AD on Dock	AD on Dock	AD on Sys	AD on Dock

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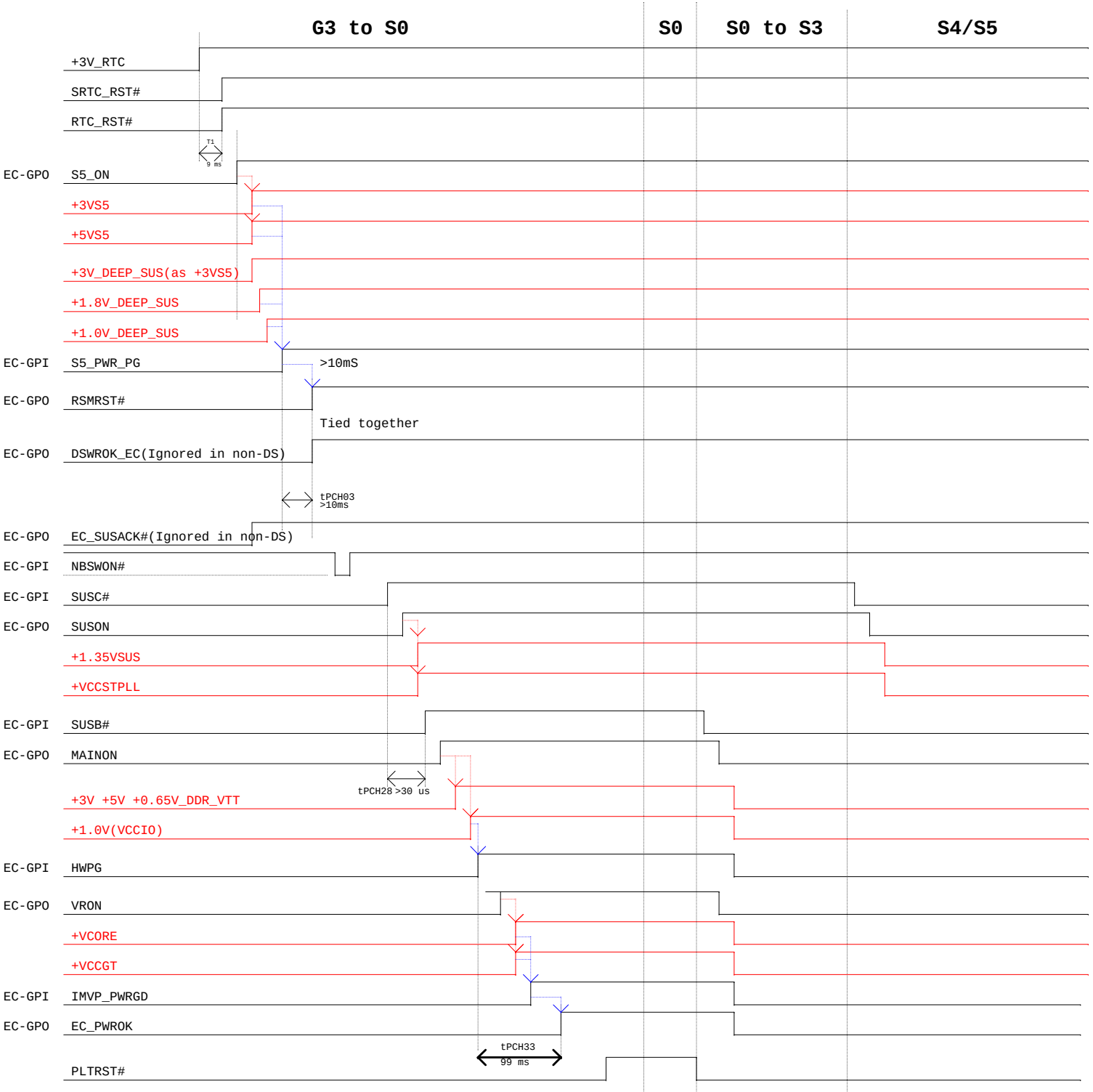

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	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
2016 FVT-STAGE	EC-FVT-01	38	05/25	R5053~R5056	Depop for colay parts
	EC-FVT-02	19	05/25	R851,R852,D27	POP R851,R852 for touch screen panel RST and reserve D27.
	EC-FVT-03	14	05/26	R197,R200	add for VPRO/Non-Vpro ID
	EC-FVT-04	16	05/26	CN3	XDP signal routing changed.
	EC-FVT-05		05/27	PJP	All PJP Change to short pad
	EC-FVT-06	42	05/27	PR272	modify 5V OCP
	EC-FVT-07	53	05/27	PQ2103,PQ2102,PR7,PR11,PR11653, PR1166,PR11678,PR11677,PQ2069, PR540, PR541, PR11635	Optimize Ideal Diode schematic
	EC-FVT-08	41	05/27	PQ2071,PL2006,PF1,PF4, Delete PD2030	For smart charge function
	EC-FVT-09	29,37	05/27	R5135~R5139,D28	Reserve to support type c dock power buttom
SIT-STAGE	EC-SIT-01	22	06/26	R316,R317	Change to 150 ohm for FSOV issue
	EC-SIT-02	13	07/01	C441,C445	Change to 12P (Vendor suggestion)
	EC-SIT-03	14,19	07/13	R5124,R5125	Add Cable ID for touch/non-touch
	EC-SIT-04	38	07/17	R5053~R5058, U5002,C9789,C9790	Default : depop VBUS protect from TPD8S300
	EC-SIT-05	38	07/17	EC6029,EC6030,U54	Change CC1/CC2 line up to 20V protect
	EC-SIT-06	24	07/25	U5004/R5145~R5149	Reserve PEDETschematic
	EC-SIT-07	21	07/25	RFID Relate Part	Remove

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